APPLICATION NOTE

Car Radio Integrated Signal Processor

TEF6890H, TEF6892H, TEF6894H

AN10106-01

Philips
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Abstract

The TEF6890H, TEF6892H and TEF6894H are monolithic BiMOS integrated circuits comprising the stereo decoder function, weak signal processing and ignition noise blanking facility for AM and FM combined with source selector and tone/volume control for AM/FM car radio applications. In addition to this the TEF6890H includes the RDS/RBDS demodulator function and the TEF6892H includes the RDS/RBDS demodulator as well as the decoder function.
The IC is I^2C bus controlled and needs no manual alignment.
No external components except (de-)coupling capacitors at signal and supply pins are necessary.

Purchase of Philips I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conforms to the I^2C specifications defined by Philips.

APPLICATION NOTE

Car Radio Integrated Signal Processor TEF6890H, TEF6892H, TEF6894H

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Summary

This report describes the function of the Car Radio Integrated Signal Processor (CRISP) series TEF6890H, TEF6892H and TEF6894H, their application and the possibilities of alignment and control via I^2C bus.

The first part of the report describes the function and features of all blocks. The second part is a detailed description of the possible settings which can be selected for different requirements and information regarding the application of the signal processor.

The application and alignments are based on a radio which uses the NICE or NICE-PACS tuner ICs.

CONTENTS

1. Introduction

The car radio integrated signal processor (CRISP) series of TEF6890H, TEF6892H and TEF6894H are monolithic BiMOS integrated circuits comprising the stereo decoder function, weak signal processing and ignition noise blanking facility for AM and FM combined with source selector and tone/volume control for AM/FM car radio applications. Furthermore TEF6890H includes an RDS/RBDS demodulator function and TEF6892H includes both RDS/RBDS demodulator and decoder. Together with a tuner IC of the NICE or NICE-PACS series TEA684xH a two-chip AM/FM radio can be realized. The interfaces of the TEF689xH series are designed for an easy connection to the NICE and NICE-PACS tuner ICs without external matching circuits. The ICs are I^2C bus controlled and need no manual alignment.

2. Functional description

The TEF6890H, TEF6892H and TEF6894H comprise the following blocks:

- Tone/Volume control
- Stereo decoder
- Ignition noise detector
- Noise blanker circuit for FM and AM
- De-emphasis and high cut circuit
- Weak signal processing; softmute, high cut control and stereo blend.
- I^2C-bus interface

The three device versions differ in their RDS/RBDS functionality:

- TEF6894H: No RDS/RBDS function
- TEF6890H: RDS/RBDS demodulator
- TEF6892H: RDS/RBDS demodulator and decoder

Except for the differences in RDS/RBDS functionality the versions are pin- and control compatible.

The block diagram of the TEF6890H is shown in Fig.1

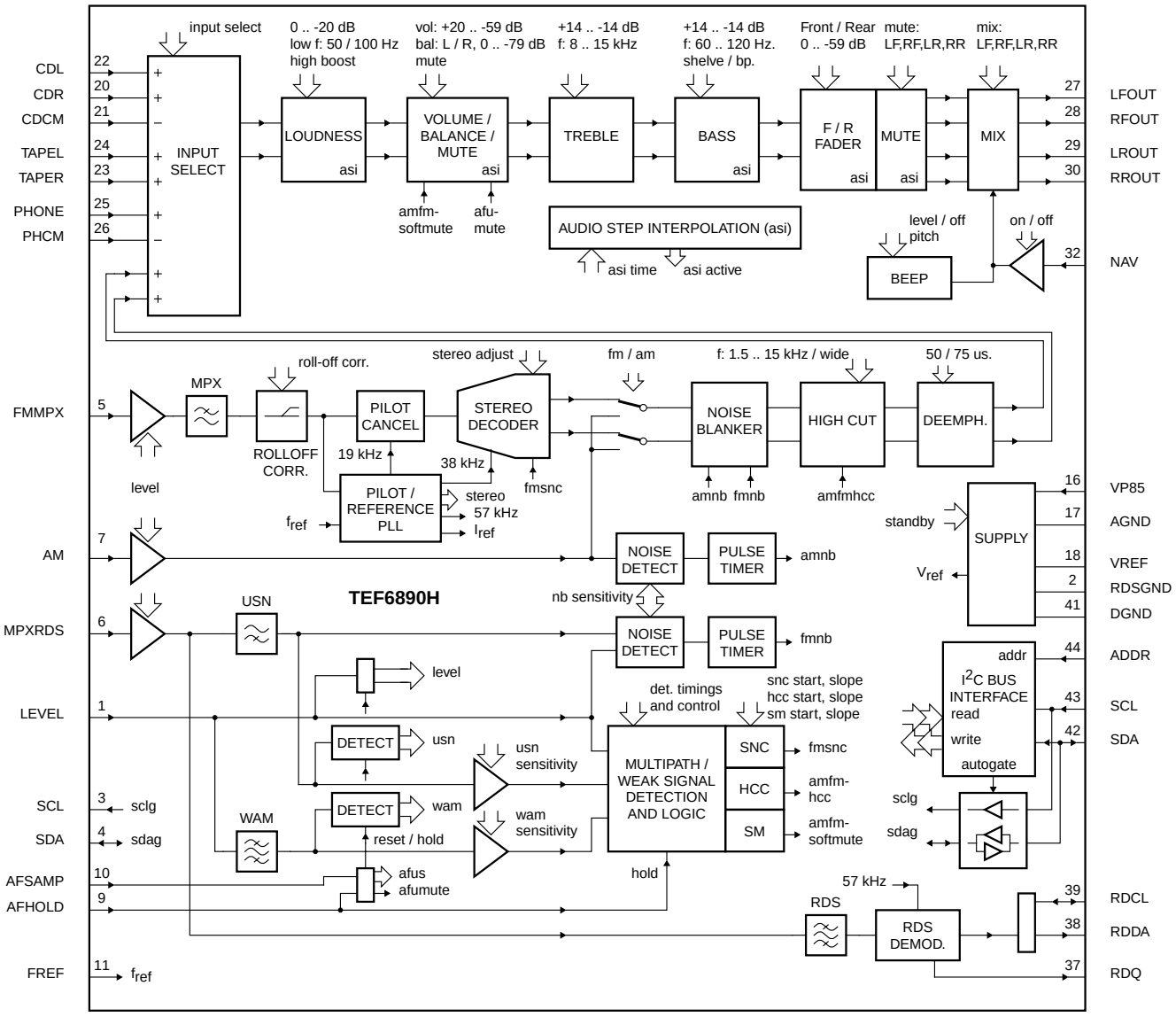

Fig.1 Block diagram

2.1 Tone volume control

2.1.1 Audio Step Interpolation, ASI

All tone volume control circuits except the treble control use the audio step interpolation, ASI. The function results in an inaudible transition from any setting of the control circuit to another one without step noise. This smooth transition is achieved by an internal circuit, which operates automatically and needs no external components. The ASI time constant during which the attenuation is changed can be selected in 4 steps by I^2C-bus. The ASI function is independent from the step size of the control. Changing the volume over ‘many’ steps takes the same time as over one step.

The ASI function becomes active when the tone volume control circuits are activated by the user to change volume- or tone-control settings and also during some functions controlled by the weak signal processing or a mute action by the AF update or Preset sequence of a NICE (TEA684xH) tuner.

2.1.2 Input selector

The input selector selects one of 4 input sources, controlled by I^2C bus:

- the radio signal from the internal FM/AM radio processing part
- a stereo signal from the CD player with ground input for suppression of common mode noise.
- a stereo signal from the tape player
- a mono signal from phone applications with ground input for suppression of common mode noise.

Input switching activates ASI muting to realize smooth input- and FM/AM -selection.

2.1.3 Loudness control

The loudness control circuit has an attenuation range from 0 to -20 dB, to be used as part of the Volume range. The step width is 1 dB at 1 kHz. Two frequencies for low boost, 50 Hz and 100 Hz, can be selected and the circuit can be used with or without high boost. The loudness control uses the ASI function.

2.1.4 Volume-, Balance- and Mute control

This circuit, which also incorporates the ASI function, is used for the volume setting by the user and for the softmute function of the weak signal processing and muting during tuning of the tuner IC. It is also used to adjust the balance of the two stereo channels. The control range of the volume control circuit is +20 dB to - 59 dB in steps of 1 dB. In combination with Loudness a control range of +20 dB to -79 dB can be realized.

2.1.5 Treble control

The treble control circuit controls the high frequency components of the audio signal in 2 dB steps in a range from +14 dB to - 14 dB. Four different treble frequencies can be selected. Since treble control does not suffer from step noise no ASI function is incorporated.

2.1.6 Bass control

The bass control sets the gain or attenuation of low frequency components in the audio signal. The step size is 2 dB and the control range is from +14 dB to - 14 dB. The bass frequency can be set to four different values. The frequency response of the bass filter can be either a shelve function or a bandpass function. Bass again uses ASI for inaudible control.

2.1.7 Fader

The next block is the fader, which is used to attenuate the front or the rear channels. The fader also includes a mute function with independent control over the four output channels. The fader has an overall control range from 0 dB to - 59 dB, with different step sizes over the whole range. Both fader and mute control use ASI.

2.1.8 Beep generator

The beep generator generates audio signals for different auxiliary purposes. The output signal is a sine wave signal. Four beep frequencies are available (500 Hz, 1000 Hz, 2000 Hz and 3000 Hz). The amplitude can be selected in 7 steps and the beep generator can be switched off by I^2C-bus.

2.1.9 Output mixer

This circuit is used to combine the 4 audio channels of the tone/volume part with the internally generated beep signal or the external NAV signal, which can for instance be generated by a navigation system. The function of the mixer circuit is controlled by I^2C-bus. The beep signal, the NAV-signal or the combination of both can be added to the audio signal in each of the four output channels. It is also possible to mute each audio channel separately and use the beep or the NAV-signal instead of the audio signals.

2.2 Radio path

The radio path comprises all the blocks from the input for the MPX signal in FM mode and the audio signal in AM mode to the input selector of the tone volume section.

2.2.1 Input amplifiers

The circuit has three inputs for the demodulated radio signals from the tuner.

The MPX signal in FM mode from the tuner is fed to the FMMPX input for the processing of the audio signals. The MPX signal is also applied to a second input, MPXRDS, for the noise blanker, the weak signal processing circuit and the RDS demodulator.
The input gain of the pair of MPX inputs can be selected in 3 settings to match the output of the RF tuner circuit. A fourth high gain setting is available for the FMMPX input for use of weather band mode in some applications.

A third input is available for the AM audio signal. The gain of this input is also variable in 3 steps.

2.2.2 FMMPX-low pass filter with roll-off correction

A low-pass filter provides the necessary signal delay for the FM noise blanker and the suppression of high frequency interferences into the stereo decoder input. The output signal of this filter is fed to the roll-off correction circuit which, together with an amplitude correction in the stereo decoder, compensates the frequency response caused by the low-pass characteristic of the tuner circuit with its IF bandpass filters. The roll-off correction circuit is adjustable in four settings to compensate different frequency response characteristics of the tuner part.

2.2.3 Stereo decoder

The MPX signal is decoded in the stereo decoder part.
A PLL regenerates the 38 kHz sub carrier from the 19 kHz stereo pilot. The fully integrated PLL oscillator is initially adjusted by a reference PLL circuit allowing instant capture for the pilot PLL mode at stereo detection. The reference PLL uses the 75.368 kHz reference frequency provided by the tuner ICs of the NICE family (TEA684xH).

The required 19 kHz and 38 kHz signals are generated by division of the oscillator output signal in a logic circuitry. The phase detector of the PLL, the pilot detector and the pilot suppression circuit are driven by the internally generated 19 kHz signals. The pilot detector circuit produces a pilot dependent voltage which switches the PLL circuit to pilot PLL mode, activates the stereo indicator bit and sets the stereo decoder to stereo mode. At the same time the detector voltage controls the amplitude of an accurate anti-phase 19 kHz signal. This anti-phase 19 kHz signal suppresses the pilot tone in the audio signal.

The MPX signal is decoded in the decoder part. The side signal (L-R) is demodulated using the generated 38 kHz signal and combined with the main signal (L+R) to get the left and right audio channel. The decoder circuit and 38 kHz signal are constructed in a special way to avoid demodulation of spurious signals of 100 kHz and 200 kHz adjacent channels. Additional roll-off compensation is done by adjusting the gain of the L-R signal in 16 fine steps. During poor RF signal conditions the FMSNC signal from the weak signal processing block has attenuation control over the L-R signal for a gradual transition from stereo to mono (stereo blend).

2.2.4 FM and AM noise blanker

The FM/AM switch selects the output signal of the stereo decoder (FM mode) or the signal from the AM input for the noise blanker block. In FM mode the noise blanker operates as a sample and hold circuit, a lowpass filter is included to suppress high frequency signals that would otherwise cause disturbance. In AM mode the audio signal is muted during the interference pulse. The different blanking actions are selected for best results with the different signal conditions.
The blanking pulse which triggers the noise blanker is generated in the noise detector block.

2.2.5 FM noise detector

The FM noise detector is used to detect noise spikes in the wanted audio signal. These noise spikes are generated as ignition noise or caused by other electric equipment in the car.

The trigger signal for the FM noise detector is derived from the MPX-signal and the LEVEL-signal. In the MPXRDS path a 4-pole high-pass filter (100 kHz) separates the noise spikes from the wanted MPX signal. Another detector circuit triggers on noise spikes on the level voltage. The signals of both detectors are combined to achieve a reliable trigger signal for the noise blanker over a large RF level range. Adaptive tresholds are created by means of an AGC circuit in the MPX and LEVEL part to control the sensitivity in relation to the average noise in the signals. This way sensitivity can be maximized while preventing false triggering. The sensitivity of the FM noise blanker can be adjusted in 4 steps for MPX and 4 steps in LEVEL.

2.2.6 AM noise detector

The trigger pulse for the AM noise blanker is derived from the AM audio signal. The noise spikes are detected by a slew rate detector, which detects excessive slew rates which do not occur in standard audio signals. The noise blanker and detector system used does not require an external or internal delay circuit. The sensitivity of the AM noise blanker can be adjusted in 4 steps.

2.2.7 High cut and de-emphasis

The high cut (HC) part is a low-pass filter circuit with dynamic and static control of the cut-off frequency.
Eight different static roll-off response curves (fixed high cut) are available via I^2C-bus, the filter curves range from no filter function down to a cut-off frequency of 1.5 kHz to match FM, AM and Weather Band signal conditions. The HC circuit also provides a dynamic control of the filter response, the HCC (high cut control). This function is controlled by the AMFMHCC signal from the weak signal processing part and reduces the filter bandwidth when weak signal conditions are detected.

The audio signal then passes the de-emphasis block with two standard de-emphasis values (50 μs and 75 μs), which can be selected via I^2C-bus, and is then fed to the input selector in the tone/volume part.

2.2.8 Weak signal processing

The weak signal processing block detects quality degradations of the incoming FM- or AM-signal and controls the processing of the audio signal accordingly to keep the subjective sound quality as high as possible given the receptions conditions.

A block diagram of the weak signal processing circuits including the noise blankers for AM and FM are shown in Fig.2

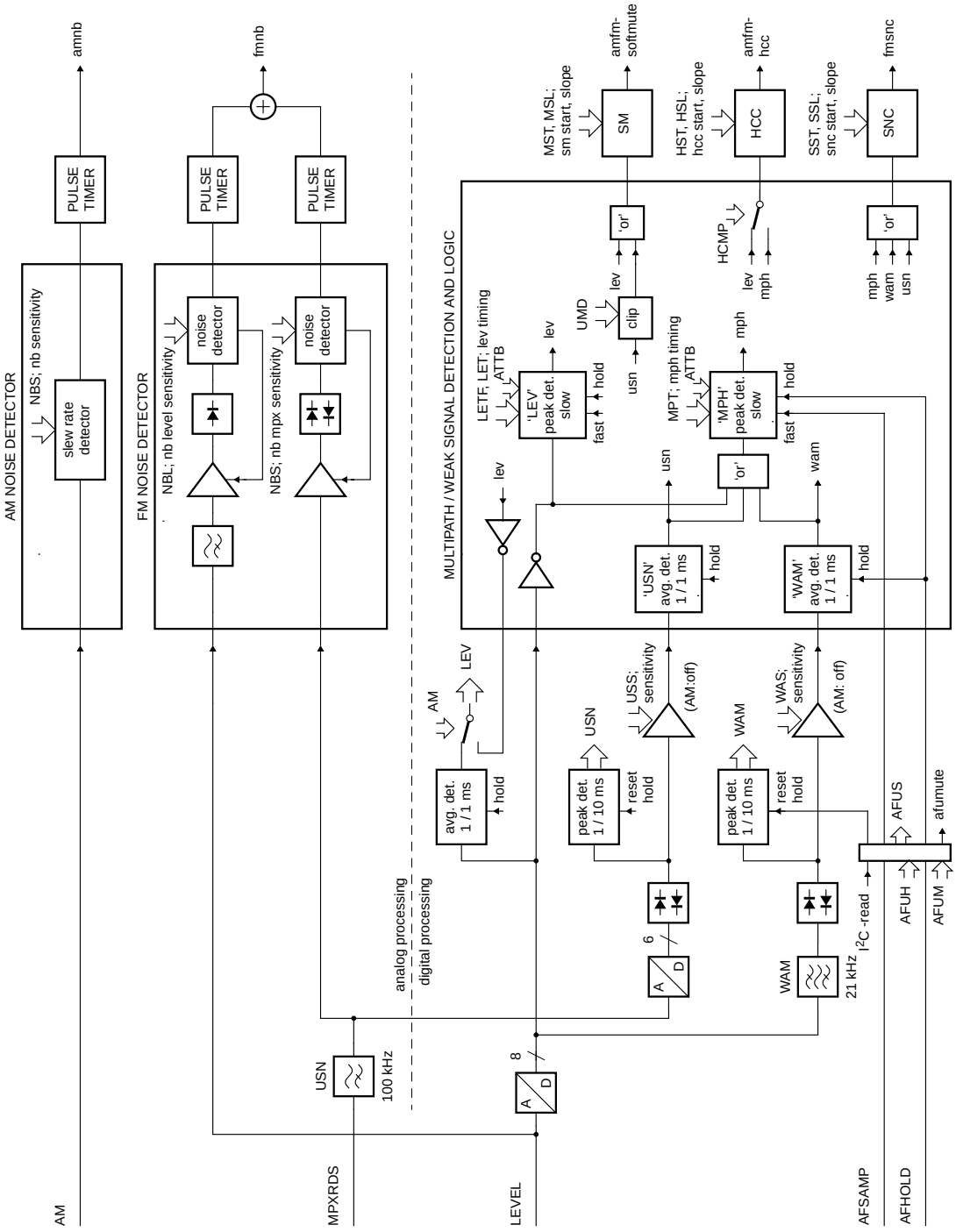

Fig.2 Block diagram of the weak signal processing

The weak signal processing block has three different quality criteria:

1. The average value of the level voltage [LEVEL]
   The level voltage is converted to a digital value by an 8-bit analog-to-digital converter.
2. The AM components on the level voltage [Wide band AM (WAM)]
   A digital filter circuit (WAM filter) derives the wide band AM components from the digital level signal.
3. The high frequency components in the MPX signal [Ultrasonic Noise (USN)].
   These components are measured with an analog-to-digital converter at the output of the 100 kHz high-pass filter in the MPXRDS path.

The values of these three signals are externally available via I^2C-bus: 8 bits for the LEVEL signal, 4 bits each for the WAM and USN signal.

In the weak signal processing block the three digital signals are combined in specific ways and via timing circuits used for the generation of control signals for soft mute, high cut control (AMFMHCC) and stereo blend (stereo noise control, FMSNC).

The sensitivities of the detector circuits WAM and USN can be selected. Also the start values and the slopes of the control functions soft mute, high cut control and stereo blend can be set via I^2C-bus. This gives a large flexibility to the radio designer and allows to match the radio to different requirements.

In AM-mode the weak signal processing is only controlled by the average value of the level voltage. For AM the weak signal processing influences the soft mute and the high cut control.

2.2.9 AF update

Soft mute, high cut control and stereo blend are put on hold during the AF updating (quality check of an alternative frequency) of the tuner. Before the AF update process starts, the current values of the weak signal processing are put on hold. After the AF update finishes the weak signal processing continues starting from these values, this way weak signal control is not influenced by AF signal conditions. During the test cycle in the AF update process (indicated by the AFSAMP signal from the NICE tuner IC) the actual quality data (LEVEL, WAM and USN) of the alternative station are measured and can be read out via I^2C-bus afterwards.

2.2.10 RDS demodulator

The RDS demodulator available in TEF6890H and TEF6892H recovers and regenerates the continuously transmitted RDS or RBDS data stream output of the multiplex signal (MPXRDS) and provides the output signals clock (RDCL), data (RDDA) and quality (RDQ) for further processing by an external RDS decoder in case of TEF6890H or the internal RDS decoder of TEF6892H. The RDS demodulator uses the stereo pilot frequency or in case of a mono signal the reference frequency (75.368 kHz) from the tuner IC and does not need a separate crystal. Direct demodulator output mode (compatible with e.g. SAA6579 and SAA6581) as well as a 16-bit buffered output mode are available.

2.2.11 RDS decoder

The RDS decoder available in TEF6892H performs the complicated tasks of syndrome detection, block synchronization, error correction and flywheel function for reliable extraction of RDS and RBDS block data. Different modes of operation can be selected to fit different application requirements. Availability of new data is signalled by read bit RDAV and output pin RDDA. Up to two blocks of data and status information are available via the I^2C-bus in a single transmission.

2.3 I²C-bus interface

The I²C-bus interface can be operated with clock frequencies up to 400 kHz and is in full compliance with the 'fast-mode' I²C specification. The I²C-bus can be operated with a supply voltage ranging from 2.5 V to 5 V.

The TEF689xH offers a gated bus interface to the tuner IC. The gate can be used to disconnect the tuner IC from the bus when no bus information is to be transmitted to the tuner. This avoids cross talk in the sensitive tuner part and thus makes the PCB layout less critical. The gate interface also allows to use 400 kHz and 100 kHz bus speed together in case the tuner IC has a 100 kHz bus interface. A supply voltage shift between main bus and tuner bus is allowed within the 2.5 V to 5 V range.

Two special control features are available for fast and easy gate control.

Shortgate: This feature activates the gate for one single transmission and automatically disconnects the gate afterwards. Shortgate is the recommended control for use with NICE TEA684xH tuner devices.

Autogate: This feature enables and disables the tuner bus automatically for a given device without the need of a specific command to the TEF689xH. Autogate offers the most convenient control but can not be used in combination with NICE TEA684xH tuners because the put forward transmission start may introduce erroneous results when reading the tuner IF counter. New tuner series will support the use of autogate.

3. The Application circuit

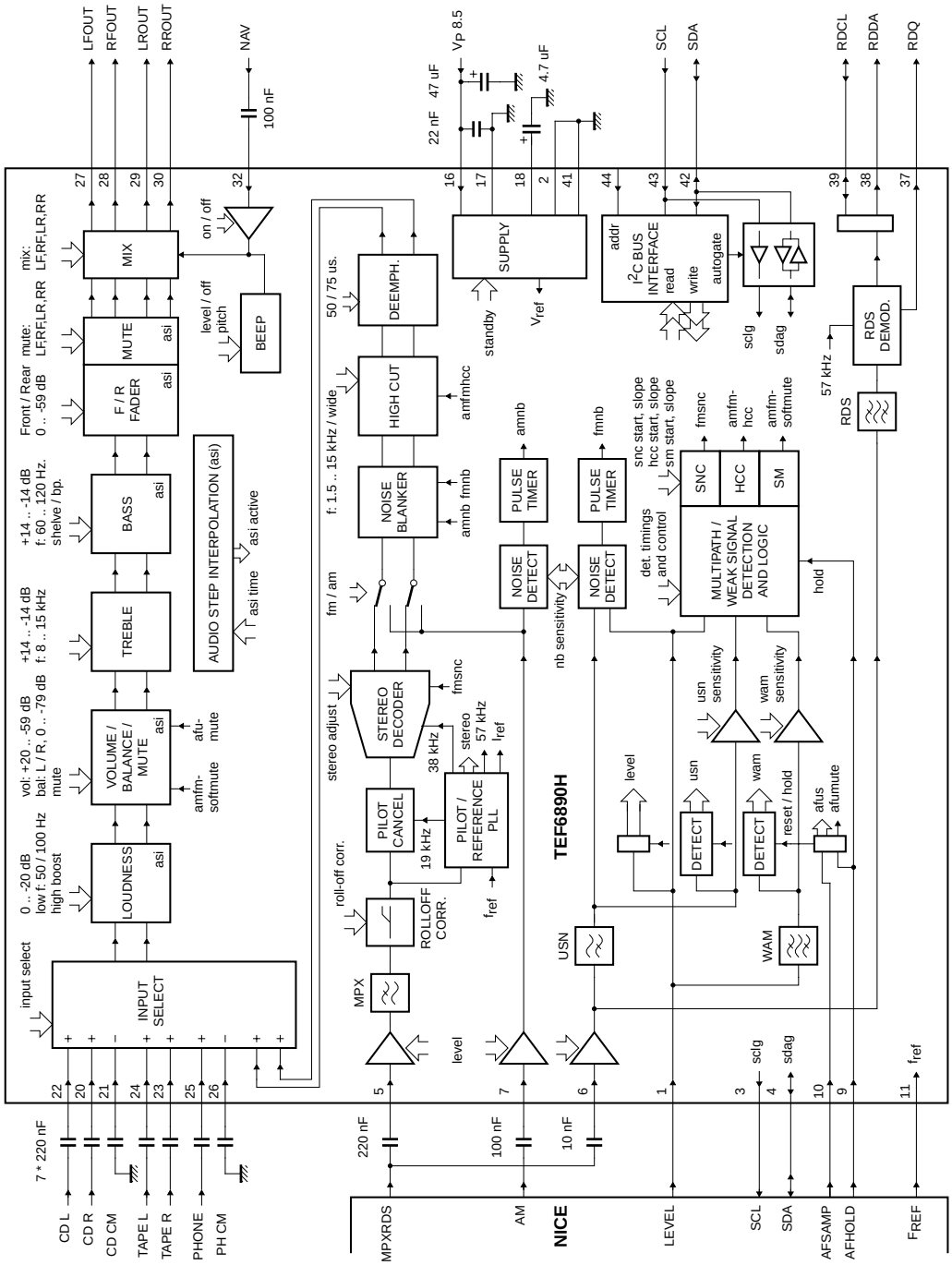

Fig.3 Application circuit

An application circuit of the TEF6890H is shown in Fig.3. The same application circuit can be used for the TEF6890H, TEF6892H and TEF6894H.

The circuit does not need any external components except for coupling capacitors for the AC signals and decoupling capacitors for the power supply. All necessary filter circuits are completely integrated and the time constants of the weak signal processing part are realized digitally.

The TEF689xH I^2C address is selected by the ADDR pin (pin 44). When grounded the address is 30H, with the ADDR pin floating the address is 32H.

3.1 Radio inputs

The interface to the tuner part is designed to fit the NICE or NICE-PACS tuners.

The AM audio output signal from the tuner is applied to the AM input of the TEF689xH via a coupling capacitor and then fed to the input of the noise blanker.

The FM-part of the TEF689xH has two input pins for the processing of the MPX output signal from the FM demodulator.
The FMMPX input (pin 5) is used for the processing of the audio signals in the stereo decoder and the tone/ volume part. The MPXRDS input (pin 6) is used as an input for the noise detector, for the weak signal processing, and for the TEF6890H and TEF6892H RDS/RBDS functions.

The AM/FM switch selects the input signal for the audio processing. The source is selected by bit AM in byte AH (RADIO). If AM = 0, the FM mode is selected (FMMPX input). If AM = 1, the AM mode is selected (AM input).

3.1.1 TEF689xH connected to the FM demodulator output

There are two possibilities for the connection of the FM inputs to the tuner.

The preferred method is displayed in Fig.3.
Both FM input pins of the TEF689xH are connected to the RDSMPX output of the NICE tuner. The RDSMPX signal is the direct output signal of the FM demodulator in the tuner IC. When this application is used the complete processing of the MPX signal is done in the TEF689xH and maximum performance is realized. During tuning and AF updating of alternative frequencies the muting is done in the volume control circuit of the TEF689xH using the ASI function to suppress audible pops. The matching of the gain in weather band reception is done by changing the gain of the FMMPX input amplifier of the TEF689xH.

3.1.2 TEF689xH connected to FMMPX and RDSMPX outputs of NICE

The muting during tuning and the matching of the weather band gain can also be done in the tuner IC. The NICE tuner ICs offer this possibility. In this case the FMMPX input of the TEF689xH has to be connected to the muted output of the NICE (FMMPX) and the MPXRDS input is connected to the NICE demodulator output (RDSMPX).

3.1.3 AFSAMP and AFHOLD input

The NICE ICs provide two automated tuning actions, AF update and Preset, which can be started via I^2C bus. Supporting functions like weak signal control and muting in the TEF689xH are controlled simultaneous by two signal lines AFHOLD and AFSAMP. The combination of NICE tuning and TEF689xH support simplifies I^2C control considerable. A detailed description of the use of NICE tuning actions and the controlled functions in TEF689xH is found in chapter “4.8 NICE tuning actions and control”.

The AFSAMP and AFHOLD input pins have pull-up functionality to connect to the open-collector outputs of NICE directly. In case the connection with NICE is not used the AFSAMP pin should be grounded.

3.1.4 FMMPX input and FM stereo channel separation

The FM stereo channel separation that can be achieved for low frequencies is limited by the value of the input capacitor at the FMMPX input pin (R_{in} = 120 kΩ). This effect is common to all stereo decoders and is introduced by the highpass filter causing phase distortion in the low frequency 'mono' signal part of the MPX signal.
An input capacitor value of 220 nF, as used in the standard application, does not limit the channel separation at 1 kHz (>> 40 dB). The degradation at lower frequencies is imperceptible to the human ear and can be disregarded, if however better figures are desired for low audio frequencies a higher input capacitor value can be used.

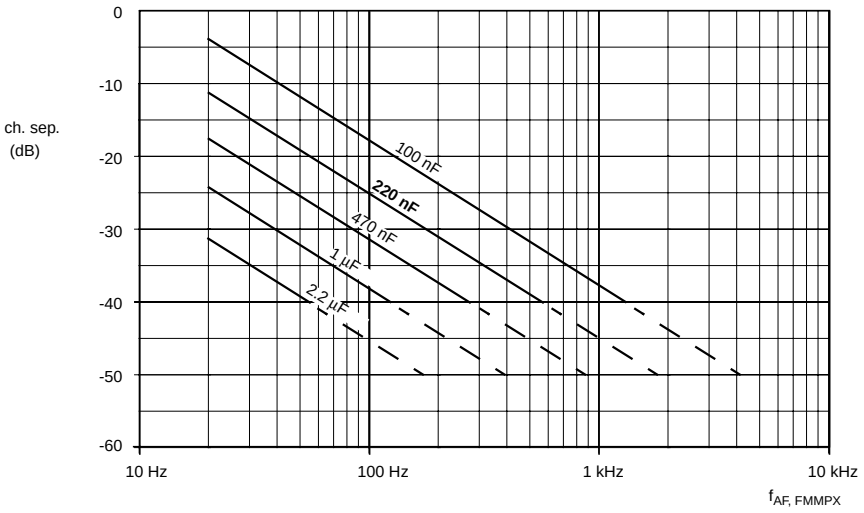

Fig.4 Influence of input capacitor value at FMMPX pin on achievable FM stereo channel separation.

When the NICE or NICE-PACS mute circuit is used an additional DC reject filter is active in the audio path set by the capacitor at pin COFFSET. For NICE (TEA6840H: pin 42, TEA6845H: pin 10, TEA6846H: pin 9) a value of 1 µF is advised and for NICE-PACS (pin 9) a value of 220 nF is recommended for good channel separation. The capacitor is of no importance when using the recommended application with the TEF689xH mute and the tuner RDSMPX output.

3.1.5 Reference frequency

The stereo decoder and the TEF6890H / TEF6892H RDS demodulator need a frequency reference to help synchronize the circuits. Furthermore for the audio filters an accurate frequency setting is desired independently of internal tolerances. The TEF689xH derives these references from a single reference frequency provided by the NICE ICs. This reference is derived from the NICE crystal oscillator frequency and has a nominal value of 20.5 MHz / 272 = 75.3676 kHz.

For stereo decoder and RDS demodulator use the reference frequency has to be present at all times. The audio filters however are set immediately after power-on and it is theoretically possible to switch off the reference frequency (i.e. the NICE tuner IC) after initial power-on. It is however advised never to use the IC without reference frequency since the reference signal from NICE is not defined when switched off and disturbances on the reference line may lead to an alignment failure.

TEF689xH indicates a power-on situation via the POR read bit, this indicator bit will return to '0' after reading but only when a reference frequency has been applied to the IC and the initial audio filter setting is completed.

3.2 Line inputs

In a car environment external audio sources may be grounded at a different point in the car than the car radio chassis. Currents flowing through the ground connection may lead to noise signals being present on the audio source ground and equally on the audio source signal line. To attenuate this kind of 'common mode' noise signals the CD and PHONE input have a common mode input that can be connected to the ground signal of the audio source. Using the difference signal between the signal line and the ground line noise signals are suppressed and a noise free audio signal is restored.

The common mode rejection achievable at the CD and PHONE inputs exceeds 40 dB. The high input impedance of the signal and common mode inputs (CDL, CDR, CDCM: R_{in} = 120 kΩ and PHONE, PHCM: R_{in} = 75 kΩ) limit the influence of external circuitry on this figure, however some application care should be taken.

If the output impedance of the CD player is 1 kΩ or higher, or when the phone impedance is 600 Ω or higher, the 40 dB figure becomes impaired. However if the output impedance is known, or can be estimated, this effect can be counteracted by inserting a resistor of the same value in series with the ground line.

Also, for good common mode rejection at low frequencies, the input capacitor values of the signal and the ground line should be sufficiently matched. The influence of capacitor tolerance and value is shown in the next figure for the CD and PHONE input pins. Also the influence of the source output impedance is indicated (when a resistor is used in the ground line it indicates the difference between the source output impedance and the ground resistor).

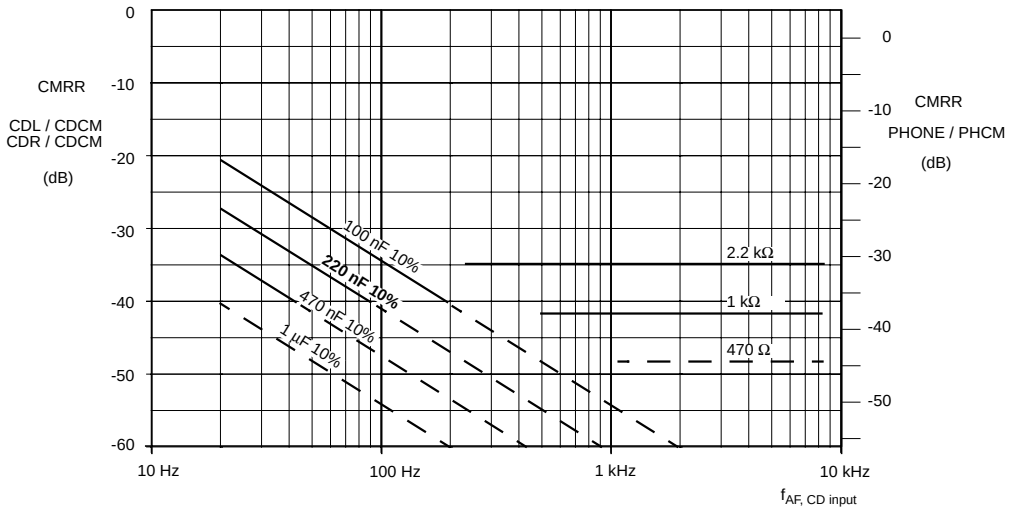

Fig.5 Influence of input capacitor value and spread and source impedance on achievable common mode rejection.

For the figure a realistic estimate of worst case capacitor to capacitor tolerance of $\sqrt{2}$ times the single capacitor tolerance is used. So C 10% denotes a situation of C -7% and C +7% at signal and ground input.
Note that the low frequency common mode rejection has a linear relation with capacitor value and tolerance, e.g. the graph line depicting 220 nF 10% also describes the situation of 100 nF 5% and 470 nF 20%.

When no common mode rejection is required for the CD or PHONE input, the CDCM or PHCM ground capacitor should be connected to the TEF689xH ground. In this case the capacitor value is not critical any more however a minimum value of 10 nF is advised to avoid deterioration of S/N and crosstalk performance.

If a signal source is not available in an application the signal and common mode input pins can be left open.

4. Settings and control

All settings of the TEF689xH are done via the I^2C-bus.
No parameter besides the bus address (30H or 32H) is determined by external components.

4.1 Gain of the input stages in the radio path

The FM input is designed for an MPX voltage of V_{MPX} = 767 mV at Δf = 75 kHz measured at an audio frequency of f_{AF} = 1 kHz. The stereo decoder, the noise blanker and the weak signal processing require the correct input amplitude.
The AM-channel requires an audio signal of V_{audio} = 967 mV at m = 100% at an audio frequency of f_{AF} = 1 kHz. The correct amplitude value is necessary for the function of the noise blanker.

The NICE ICs provide the required input voltage for the TEF689xH without any correction.
For applications with other tuners or non-standard tuner applications of the NICE the input gain of the FM and AM channel of the TEF689xH can be increased by 3 dB or 6 dB.

For weather band reception the gain of the FMMPX input can be set to 23.5 dB to compensate the low frequency deviation of weather band transmitters.

The setting of the input gain is done by the bits ING1 and ING0 in byte AH (RADIO)

TABLE 1 Setting of the input gain, byte AH

APPLICATION	GAIN FOR FMMPX INPUT (dB)	GAIN FOR MPXRDS AND AM INPUT (dB)	ING1	ING0
NICE tuner	0	0	0	0
Non standard application or other tuner	3	3	0	1
	6	6	1	0
weather band reception	23.5	0	1	1

4.2 Roll off correction of the FM channel

The frequency response of the MPX signal from the tuner is not flat because of the bandpass characteristic of the IF filters. This reduces the amplitude of the stereo component (L - R) at 38 kHz in the MPX signal. For optimum stereo channel separation this influence has to be compensated by the roll off correction and the stereo adjust. The roll off correction influences the frequency response of the input filter and is used as a coarse alignment of the channel separation. It is aligned by the bits CSR1 and CSR0 in byte 5H (CS ALIGN).
A fine alignment of the channel separation is possible by aligning the gain of the stereo component (L - R) in the stereo decoder block. This is done by setting the bits CSA3 to CSA0 in byte 5H.

4.3 Stereo Decoder

When a stereo signal is received, the pilot signal (19 kHz) is detected and stereo function is indicated by bit STIN in read byte 1. With a pilot signal STIN = 1.

It is possible to set the receiver to mono when a stereo signal is received. This is done by the MONO bit in byte AH (RADIO). If MONO = 1, the stereo decoder is set to FM mono, the STIN indication however is not influenced.

4.4 Noise detector

The FM noise detector uses the high frequency components in the MPX and the level signal for the detection of noise spikes. The level of these high frequency components depends on the gain and the IF filter response of the tuner. Therefore the sensitivity of the noise detector circuits of the TEF689xH can be adjusted to match the characteristics of the tuner. The optimum setting is a compromise between maximum sensitivity to the noise spikes and least false triggering on other noise sources. Both level and MPX sensitivity can be selected independently.

In the AM noise detector the slew rate of the audio signal is the criterion for the detection. The slew rate is also dependent on characteristics of the tuner, for instance on the IF filter bandwidth. Therefore also the AM noise detector sensitivity can be adjusted.

The same bits are used for the adjustment of the FM MPX noise detector and the AM noise detector.

TABLE 2 Setting of the noise blanker sensitivity, byte AH

MPX SENSITIVITY OF FM NOISE BLANKER (mV_{PEAK})	SENSITIVITY OF AM NOISE BLANKER (%)	NBS1	NBS0
10	110	0	0
20	140	0	1
50	175	1	0
100	220	1	1

TABLE 3 Setting of the noise blanker sensitivity, byte BH

LEVEL SENSITIVITY OF FM NOISE BLANKER (mV_{PEAK})	NBL1	NBL0
110	0	0
120	0	1
150	1	0
200	1	1

4.5 High cut (Fixed High Cut)

The high cut function has two components. A fixed setting (fixed high cut) and an adaptive setting (high cut control) controlled by the weak signal processing block. The fixed setting defines a maximum audio bandwidth to the weak signal high cut control. To realize an effective action the high cut function is not realized by shifting of the de-emphasis filter but by use of a stand alone low pass filter circuit.

One out of eight fixed high cut settings can be selected by the bits HCF2 to HCF0 in byte 8H. The possible frequency response curves of fixed high cut are displayed in Fig.6
As an indication of application use fixed high cut values between unlimited and 6.8 kHz may be used for FM, between 6.8 kHz and 3.3 kHz for AM and for weather band 2.2 kHz or 1.5 kHz may be a good choice.

For a description of the weak signal processing high cut control see chapter “4.7.5.2 High cut control”.

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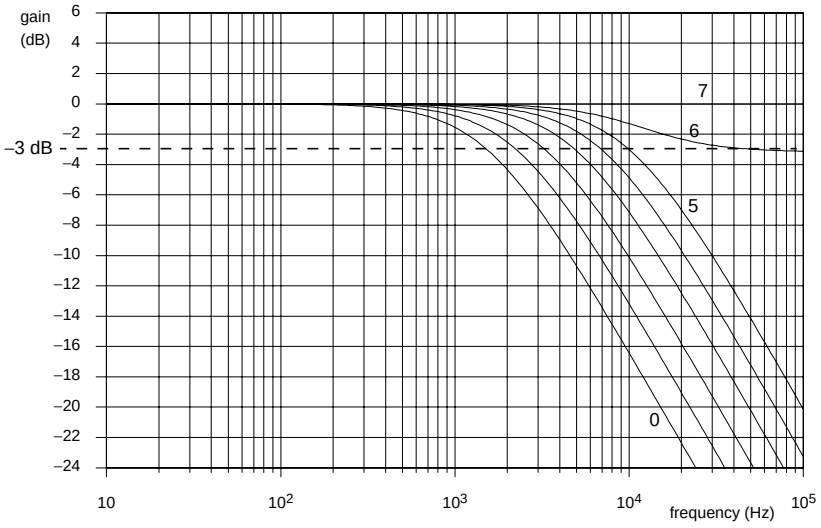


Fig.6 Setting of the fixed high cut control

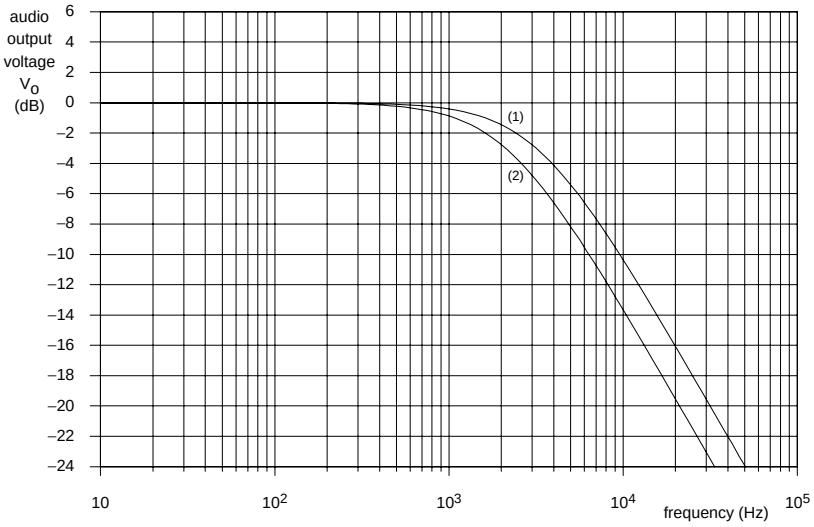
The indicated maximum bandwidth of the settings is the cut off frequency at α = -3 dB

TABLE 4 Setting of the fixed high cut control, byte 8H

B_{max} (kHz)	HCF2	HCF1	HCF0	CURVE
1.5	0	0	0	0
2.2	0	0	1	1
3.3	0	1	0	2
4.7	0	1	1	3
6.8	1	0	0	4
10	1	0	1	5
Wide	1	1	0	6
Unlimited	1	1	1	7

4.6 De-emphasis circuit

After the high cut control circuit the audio signals pass the de-emphasis circuit. This circuit is a single pole low pass filter which compensates the pre-emphasis that is applied to the radio signal in the transmitter. Two standards of the de-emphasis value exist: 50 μs (Europe / Japan) and 75 μs (USA). The time constant can be selected by bit DEMP in byte AH (RADIO). The de-emphasis time constant is 75 μs with DEMP = 0 and DEMP = 1 selects the de-emphasis time constant of 50 μs; see Fig.7
The time constant is defined without external components.



(1) τ = 50 μs

(2) τ = 75 μs

Fig.7 De-emphasis curves for τ = 50 μs and τ = 75 μs

4.7 Weak signal processing

The weak signal processing circuit controls softmute, high cut control and stereo blend depending on the signal quality. The signal quality is determined by the average level voltage (LEVEL), the high frequency components in the MPX signal (USN, ultrasonic noise) and AC components on the level signal (WAM, wide band AM).

For the correct function of the weak signal processing circuit it is necessary to apply the required MPX amplitude to the MPXRDS input.

4.7.1 Level voltage

The level curve which is applied to the LEVEL input of the TEF689xH should be adjusted to a curve as displayed in Fig.8. This assures that the start levels of stereo blend, softmute and high cut can be set to the required values and that internal thresholds in the weak signal processing are set to the optimum values.
The level voltage is about 0.5 V when no RF signal is applied. The slope should be 800 mV/20 dB.
In the NICE tuners the level voltage can be adjusted by the level DAA part, which controls offset and gain of the level detector circuit.

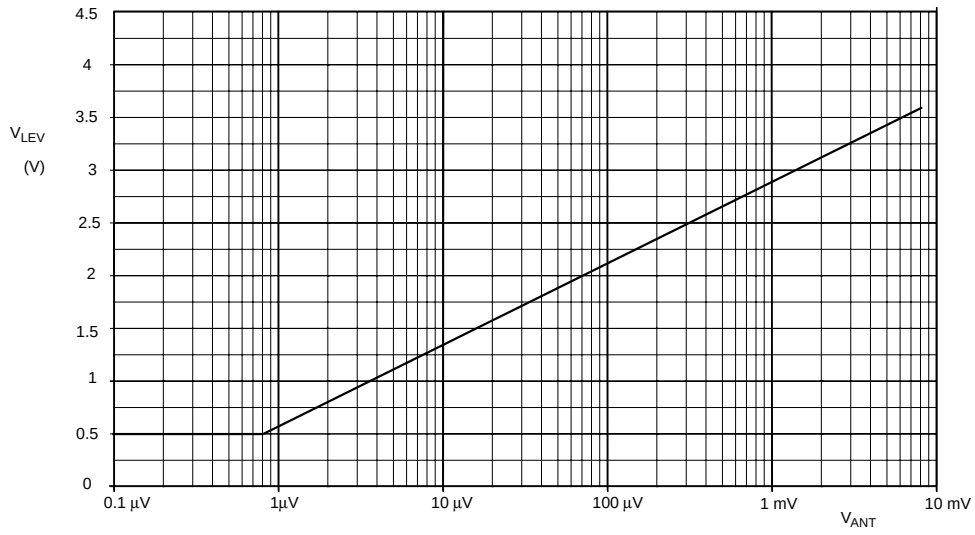


Fig.8 Expected level curve from the tuner

The level voltage is converted to a digital value in an 8 bit A to D converter. This digital value can be read out by the I^2C bus and is also used as an input value for the weak signal processing circuit.

4.7.2 The wide band AM signal WAM

The digitized level signal is filtered by a digital 21 kHz bandpass filter to generate the WAM signal, which contains the AC component of the level signal. There is no WAM signal at good RF receiving conditions. At multipath conditions the level signal is amplitude modulated and the WAM signal indicates the magnitude of the multipath signal. The WAM amplitude can be read out via I^2C bus. The WAM signal is also used as an input for the weak signal processing. The gain in the WAM path can be set to four different values. This changes the WAM sensitivity of the weak signal processing in four steps.

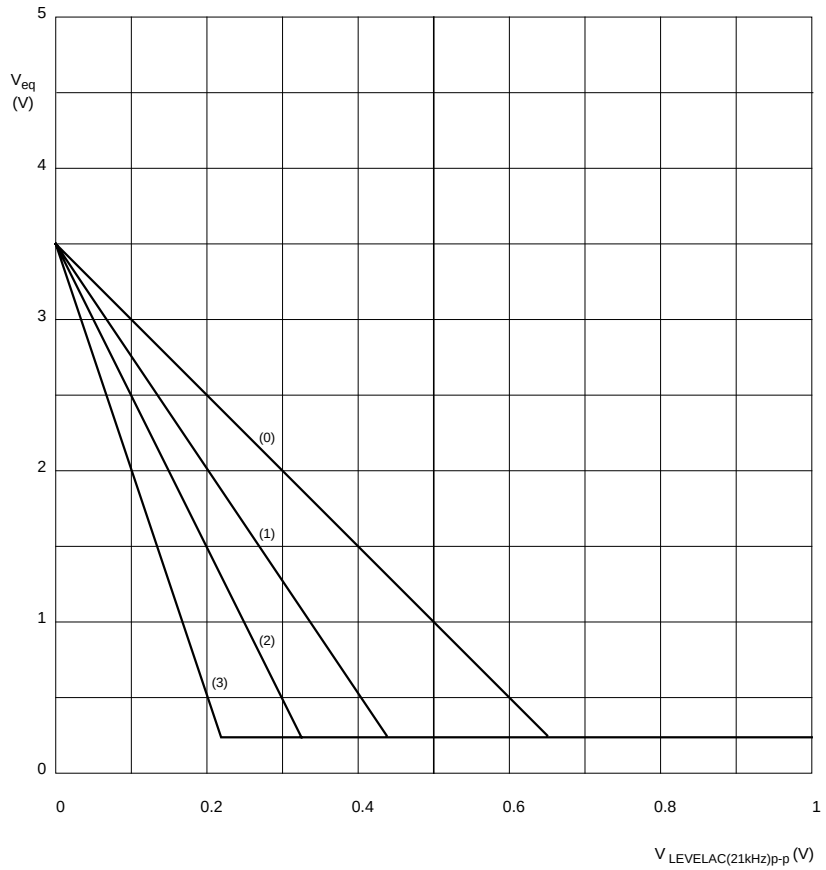


Fig.9 Equivalent level Voltage V_{eq} versus level AC input at 21 kHz

Fig.9 shows the equivalent level voltage V_{eq} versus the AC voltage at 21 kHz on the level voltage.

The expression “equivalent level voltage” is used to explain the weak signal control effect that is caused by the WAM signal: The equivalent level voltage is that level voltage which causes the same softmute, stereo blend and high cut control as the corresponding WAM signal. This expression is also used for the definition of the USN signal.

The four sensitivity values can be set by the bits WAS1 and WAS0 in byte 6H (MULTIPATH).

TABLE 5 Setting of the WAM sensitivity, byte 6H

WAS1	WAS0	WIDE BAND AM CONTROL SENSITIVITY
0	0	(0): –2 V/0.4 V
0	1	(1): –3 V/0.4 V
1	0	(2): –4 V/0.4 V
1	1	(3): –6 V/0.4 V

4.7.3 The ultrasonic noise signal USN

The MPXRDS signal passes an analog 4-pole high pass filter with a cut off frequency of 100 kHz. The output signal of this filter, the USN signal, is used in the FM noise detector circuit for the detection of noise spikes and in the weak signal processing circuit for the detection of multipath and adjacent channel interferences. The USN signal is converted into a digital value in an A to D converter. This value can be read out as a 4 bit value via I^2C bus. The USN value is also applied to the weak signal processing circuit where the gain can be adjusted in four steps to vary the sensitivity of the USN part. The four sensitivity values are shown in Fig.10

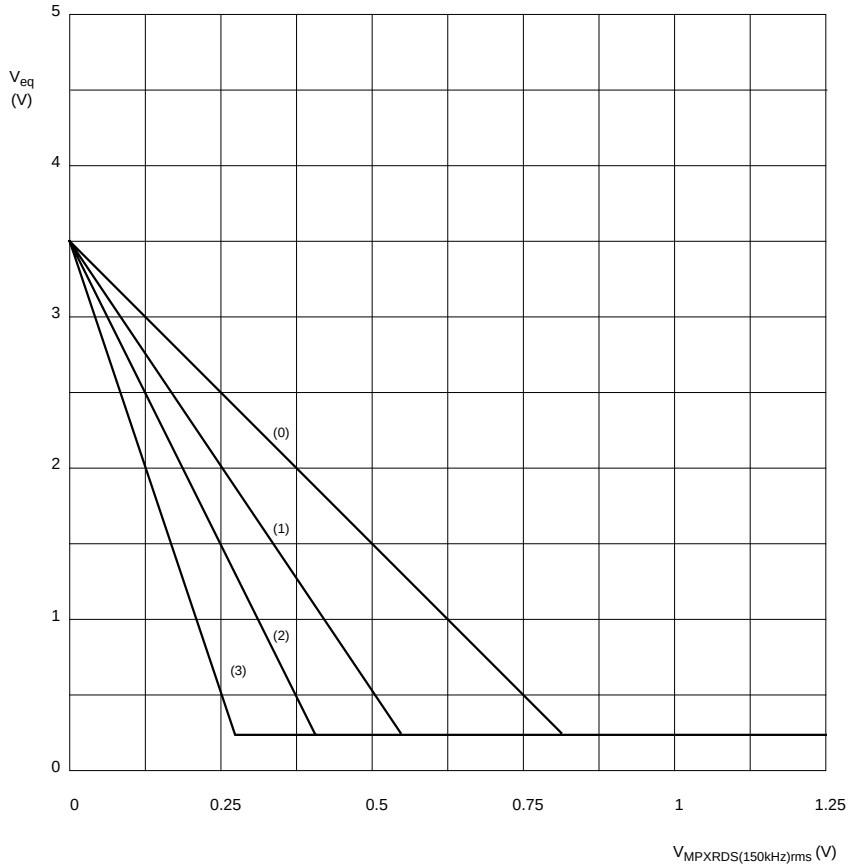


Fig.10 Equivalent level voltage V_{eq} (USN and MPH detector) versus MPX signal at 150 kHz

The sensitivity values are selected by the bits USS1 and USS0 in byte 6H (MULTIPATH).

TABLE 6 Setting of the USN sensitivity, byte 6H

USS1	USS0	ULTRASONIC NOISE CONTROL SENSITIVITY
0	0	(0): –2 V/0.5 V
0	1	(1): –3 V/0.5 V
1	0	(2): –4 V/0.5 V
1	1	(3): –6 V/0.5 V

4.7.4 Detector circuits

The processing part consists of detector circuits which combine the three input signals LEVEL, WAM and USN with specific timing circuits for optimum suppression of interferences.

4.7.4.1 Level detector

The LEVEL value is weighted in the LEV detector. The LEV detector has 8 timing sets, which can be selected by I^2C bus. The time constants of this detector are shown in Table 7

TABLE 7 Attack- and Decay times of the LEVEL detector, data byte 4H and data byte 6H

$T_{LEVEL,ATTACK}$ (s)	$T_{LEVEL,DECAY}$ (s)	LETF	LET1	LET0
3	3	0	0	0
3	6	0	0	1
1.5	1.5	0	1	0
0.5	1.5	0	1	1
0.5	0.5	1	0	0
0.17	0.5	1	0	1
0.06	0.17	1	1	0
0.06	0.06	1	1	1

The output value of this detector is the lev-signal, which is used to generate the SM (softmute) output signal and optional the HCC (high cut control) output signal.

4.7.4.2 WAM- and USN detectors

The signals WAM and USN are weighted in fast average detectors with a fixed attack and decay time of 1 ms. The output signals are wam and usn. The usn signal can have direct control over SM (softmute) and both wam and usn can have direct control over SNC (stereo blend), furthermore these signals are input for the slow MPH detector.
In AM mode no functional WAM or USN signal is available and the WAM and USN detectors are switched off.

4.7.4.3 Multipath (MPH) detector

The three signals lev, wam and usn are combined in a multi-valued “or” function. This means that the highest of these three values controls the MPH detector. The two other values have no influence on the circuit. The output value is the mph signal generating SNC and optional HCC control. The MPH detector has 4 sets of attack- and decay times, which are selected by I^2C bus.

TABLE 8 Attack- and Decay times of the MPH detector, byte 6H

$T_{MPH,ATTACK}$ (s)	$T_{MPH,DECAY}$ (s)	MPT1	MPT0
0.5	12	0	0
0.5	24	0	1
0.5	6	1	0
0.25	6	1	1

4.7.4.4 Fast time constants of LEVEL detector and MPH detector

In some cases the LEVEL and MPH time constants are too slow for a sufficient weak signal processing. When the radio is tuned to another station, it is required that the weak signal processing follows the new conditions much faster than the standard attack times in the continuous weak signal processing. During a Preset change of NICE the LEVEL and MPH time constants are automatically set to the fast mode of 60 ms but the same function is also available via the SEAR bit in byte AH (RADIO). The fast time constant of 60 ms attack and decay time is selected for both detectors when SEAR = 1.

4.7.5 Control circuits

The weak signal processing circuit has 3 control outputs

- SNC for the stereo blend function, this controls the stereo decoder part
- HCC for the high cut control, this controls the high cut circuit
- SM for the softmute function, this controls the volume control part

The input signals for these three circuits are derived from the output values of the detectors.

- the input for the SNC is the highest value of the slow mph, fast wam or fast usn signal (“or” function)
- the input for the HCC can be selected by the bit HCMP in byte 7H (SNC).
  If HCMP = 0, the high cut control is only controlled by the slow lev signal from the level (LEV) detector.
  If HCMP = 1, the high cut control is controlled by the slow mph signal from the multipath (MPH) detector.
- the input for SM is the highest value of the slow lev or fast usn signal (“or” function). The mute depth caused by usn can be limited in 4 steps which are selected by I^2C bus. This function is described together with the softmute function in section “Softmute” on page 29.

In the three blocks SNC, HCC and SM the control values for the stereo blend, high cut control and softmute are generated. These circuits offer high flexibility for the specific requirements of the radios. The control functions stereo blend, high cut and soft mute depend on the output values of the detector and timing circuits. To indicate the control effect of the wam and usn values they are described as “equivalent level voltage”. The start and slope values of the control functions can be varied by I^2C bus in a wide range offering a good selection range for FM as well as AM radio.

4.7.5.1 Softmute

Three parameters of the softmute control can be adjusted by I^2C bus, the start level of the muting, the steepness of the slope and the mute depth caused by USN. The softmute can be disabled by the bit SMON in byte 9H (SOFTMUTE). If SMON = 0, the soft mute function is disabled.

Fig.11 shows the settings of the mute start level, which can be set to 8 different values.
The 8 values are displayed for a slope setting of MSL = 3, two curves are shown for MSL = 0.

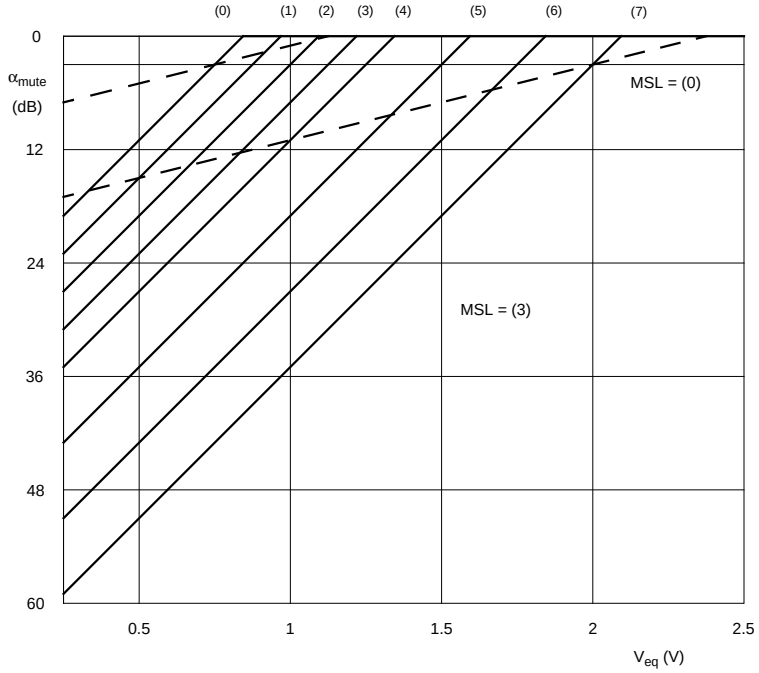


Fig.11 Soft mute start

The bits MST2 to MST0 define the equivalent level voltage at which α_{mute} = 3 dB

TABLE 9 Soft mute start, byte 9H

MST2	MST1	MST0	EQUIVALENT LEVEL OF SOFT MUTE START (α_{mute} = 3 dB)
0	0	0	(0): 0.75 V
0	0	1	(1): 0.88 V
0	1	0	(2): 1 V
0	1	1	(3): 1.12 V
1	0	0	(4): 1.25 V
1	0	1	(5): 1.5 V
1	1	0	(6): 1.75 V
1	1	1	(7): 2 V

The soft mute slope can be selected in 4 steps as shown in Fig.12

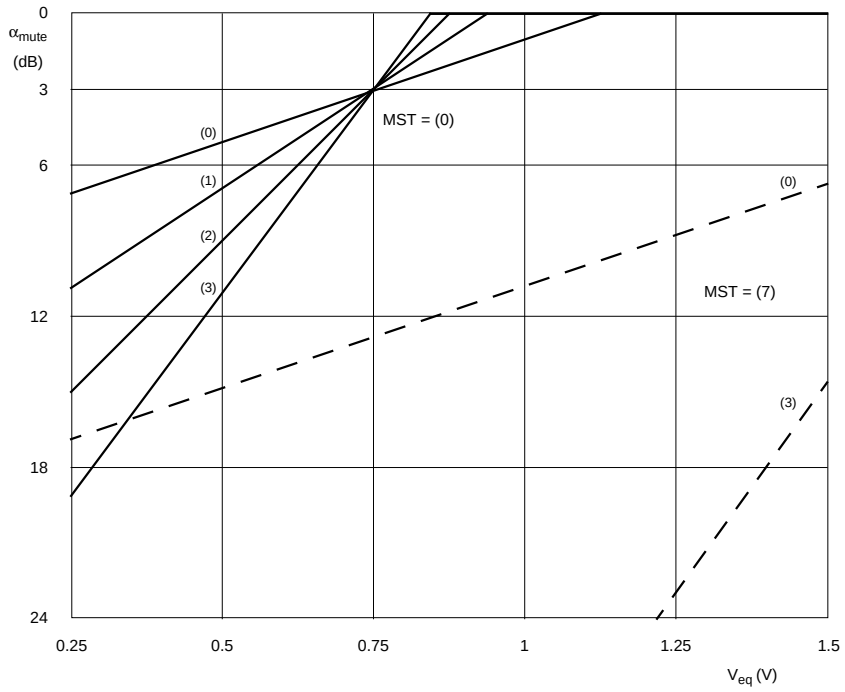


Fig.12 Soft mute slope

The four settings with MST = 0 and 2 settings with MST = 7 are shown.

TABLE 10 Soft mute slope, byte 9H

MSL1	MSL0	SOFT MUTE SLOPE (α_{mute}/EQUIVALENT LEVEL VOLTAGE)
0	0	(0): 8 dB/V
0	1	(1): 16 dB/V
1	0	(2): 24 dB/V
1	1	(3): 32 dB/V

The maximum mute depth, which is caused by ultrasonic noise can be limited to four values which are selected as displayed in Fig.13.

The soft mute, which is caused by the average level voltage is not limited by this function.

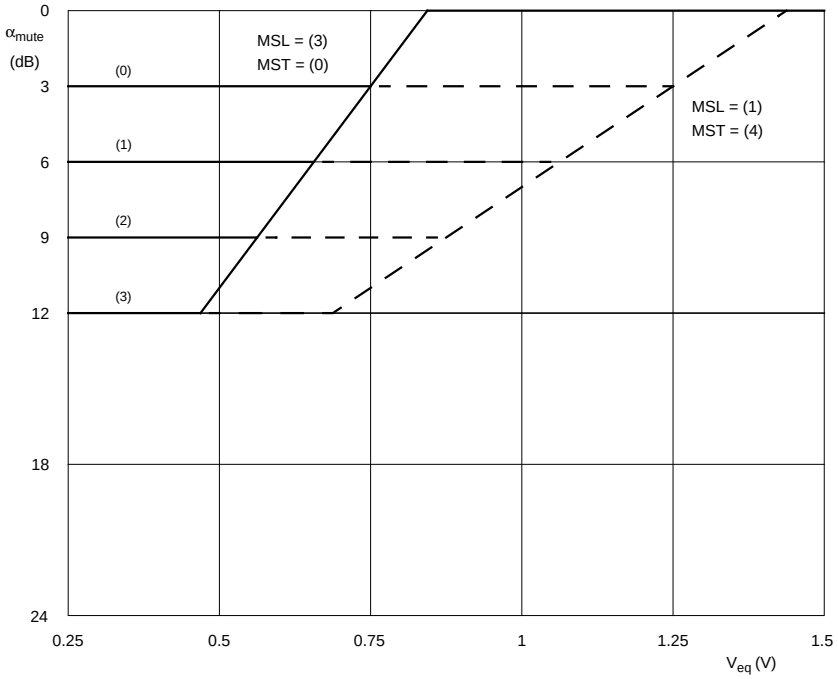


Fig.13 Soft mute depth

TABLE 11 Maximum soft mute depth caused by USN, byte 9H

UMD1	UMD0	SOFT MUTE DEPTH CAUSED BY ULTRASONIC NOISE
0	0	(0): 3 dB
0	1	(1): 6 dB
1	0	(2): 9 dB
1	1	(3): 12 dB

4.7.5.2 High cut control

This function reduces the cut off frequency starting at the fixed setting of the high cut filter (see chapter “4.5 High cut (Fixed High Cut)”) during conditions of poor signal quality. As in the other weak signal processing functions the start value and the slope of the high cut control can be selected. There are 8 start settings. The start value is that equivalent level voltage at which the amplitude of a high frequency audio signal starts decreasing.
The start value of the dynamic high cut control is selected with bits HST2 to HST0 in byte 8H. 8 settings are possible.

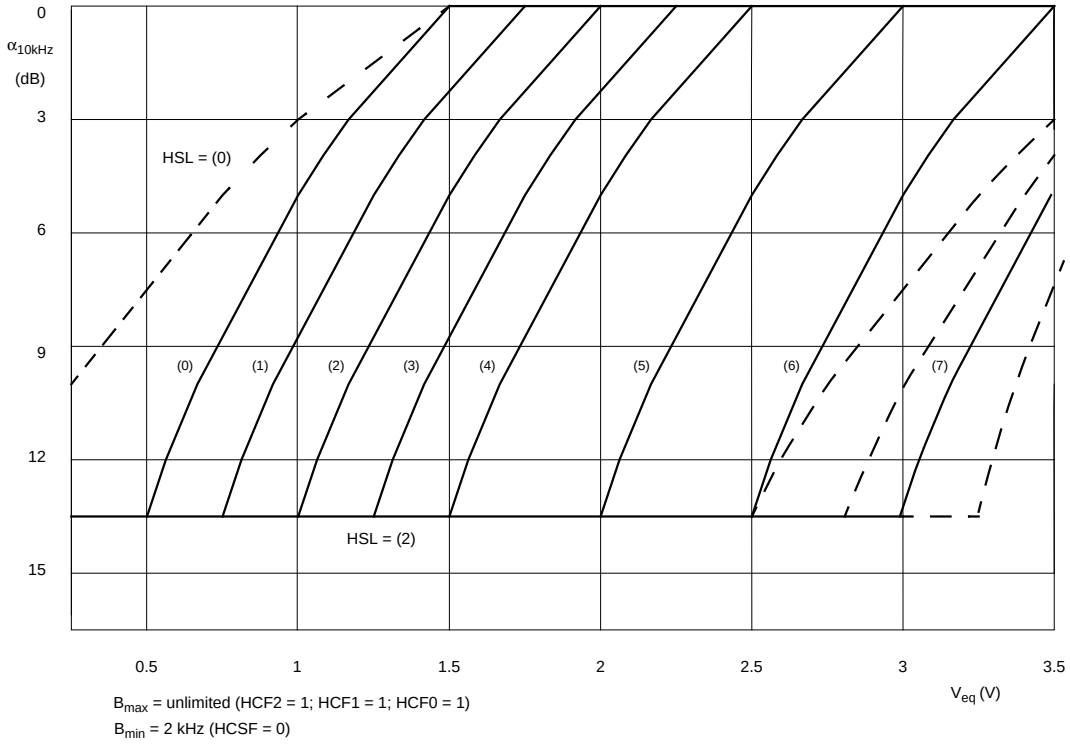


Fig.14 High cut control start settings

As an indication of high cut control the attenuation of an audio frequency of 10 kHz is used.

TABLE 12 Start of high cut control, byte 8H

HST2	HST1	HST0	EQUIVALENT LEVEL VOLTAGE AT HIGH CUT CONTROL START
0	0	0	(0): 1.5 V
0	0	1	(1): 1.75 V
0	1	0	(2): 2 V
0	1	1	(3): 2.25 V
1	0	0	(4): 2.5 V
1	0	1	(5): 3 V
1	1	0	(6): 3.5 V
1	1	1	(7): 4 V

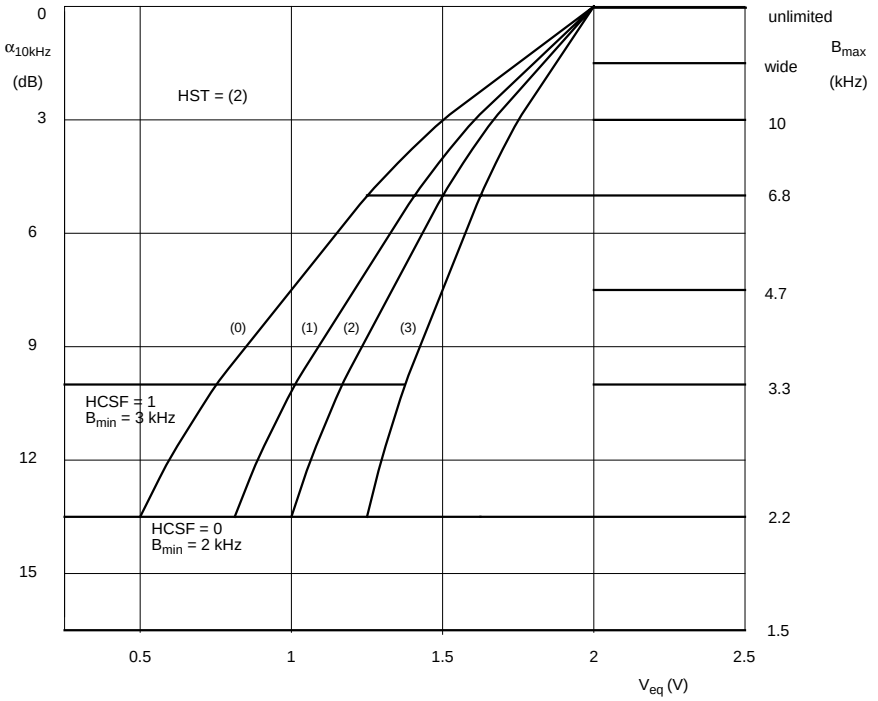


Fig.15 High cut control slope settings

The slope can be selected in 4 steps. Fig.15 shows the attenuation of an audio signal of 10 kHz. Depending on the setting of the fixed high cut, the attenuation starts at different fixed values. These values are indicated on the right edge of the diagram. The displayed curve shows the attenuation versus equivalent level voltage for the setting: B_{max} = unlimited.

TABLE 13 Setting of the high cut control slope, byte 8H

HSL1	HSL0	HIGH CUT CONTROL SLOPE (α_{10kHz}/EQUIVALENT LEVEL VOLTAGE)
0	0	(0): 9 dB/V
0	1	(1): 11 dB/V
1	0	(2): 14 dB/V
1	1	(3): 18 dB/V

When a high fixed cut off frequency or a flat frequency response is selected it may be desired to limit the dynamic high cut control. This keeps the difference in the frequency response smaller when the high cut action starts. Therefore it is possible to limit the high cut control function to a minimum cut off frequency of 3 kHz. This is selected by the bit HCSF in byte 7H.

TABLE 14 Setting of the HCC minimum bandwidth

HCSF	MINIMUM BANDWIDTH
0	2.2 kHz
1	3.3 kHz

The maximum attenuation in each setting depends on the setting of the minimum cut off frequency. The two values for B_{min} = 2.2 kHz and B_{min} = 3.3 kHz are indicated in Fig.15.

4.7.5.3 Stereo blend

The stereo blend function is adjusted in 16 steps for the SNC start value and 4 steps for the slopes of stereo blend. The start value is that equivalent level voltage, at which the channel separation starts decreasing. This is displayed in Fig.16 for 4 typical start values with a slope of SSL = 2. The dashed lines show the curve with the lowest start value and the slope SSL = 0 and the curve with the highest start value with a slope value SSL = 3.

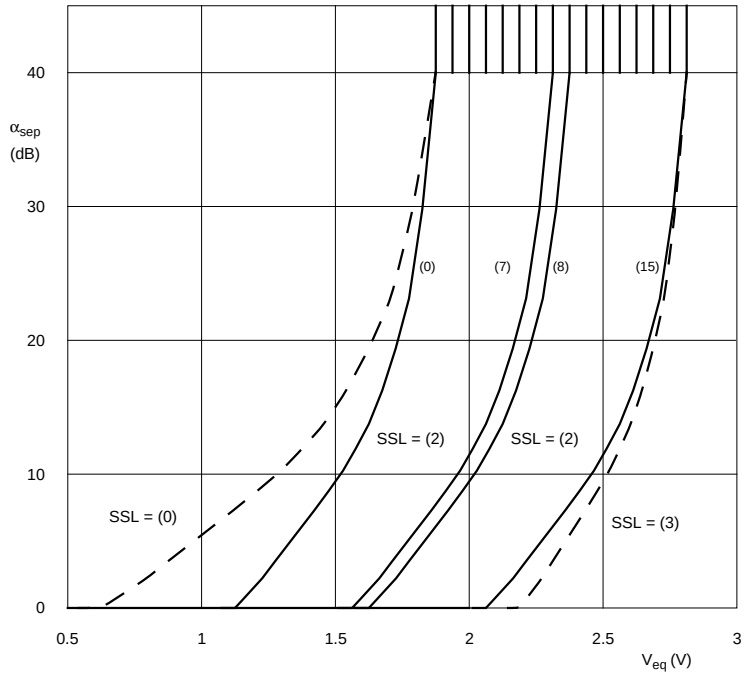


Fig.16 Stereo blend (Stereo noise control, SNC) start value versus equivalent level voltage

The values for the start level are listed in the table

TABLE 15 start levels of stereo blend, byte 7H

SST3	SST2	SST1	SST0	EQUIVALENT LEVEL VOLTAGE AT STEREO NOISE CONTROL START
0	0	0	0	(0): 1.88 V
0	0	0	1	(1): 1.94 V
0	0	1	0	(2): 2 V
0	0	1	1	(3): 2.06 V
0	1	0	0	(4): 2.13 V
0	1	0	1	(5): 2.19 V
0	1	1	0	(6): 2.25 V
0	1	1	1	(7): 2.31 V
1	0	0	0	(8): 2.38 V
1	0	0	1	(9): 2.44 V
1	0	1	0	(10): 2.5 V
1	0	1	1	(11): 2.56 V

SST3	SST2	SST1	SST0	EQUIVALENT LEVEL VOLTAGE AT STEREO NOISE CONTROL START
1	1	0	0	(12): 2.63 V
1	1	0	1	(13): 2.69 V
1	1	1	0	(14): 2.75 V
1	1	1	1	(15): 2.81 V

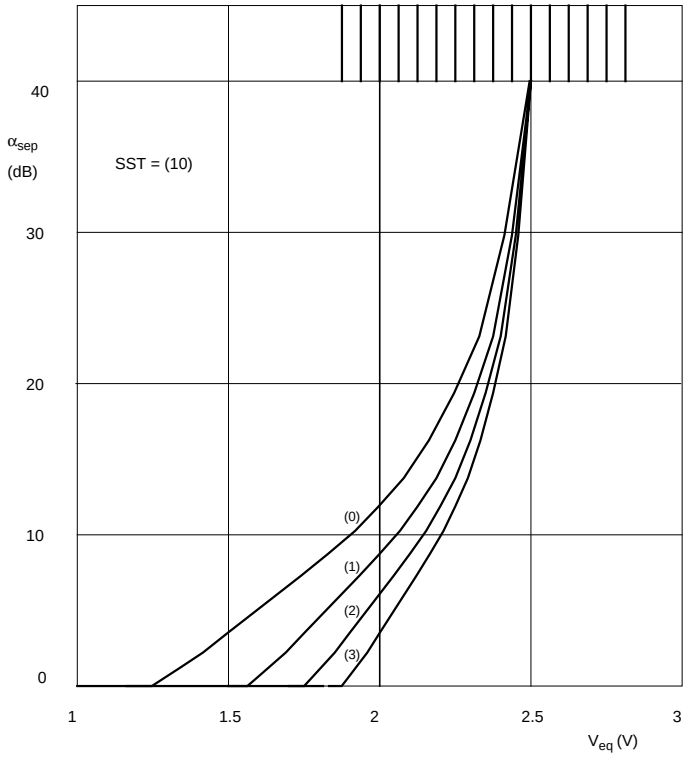


Fig.17 Stereo blend slope value versus equivalent level voltage

Fig.17 shows the four settings of the slope with the start value SST = 10

TABLE 16 slope values of stereo blend, data byte 7H

SSL1	SSL0	STEREO NOISE CONTROL SLOPE (α_{sep}/EQUIVALENT LEVEL VOLTAGE)
0	0	(0): 38 dB/V
0	1	(1): 51 dB/V
1	0	(2): 63 dB/V
1	1	(3): 72 dB/V

4.7.6 Fast weak signal attack start via ATTB option

Normally the LEV and MPH detectors follow the input signals of LEVEL (and WAM and USN) over their complete range. However in the situation of a sudden signal degradation of a good signal condition this introduces a delay in the attack of actual weak signal control because it takes time for the detectors to reach the control range of the different controls. This delay can be minimized of course by using a faster attack time however this may lead to undesired behaviour in other situations.

Instead the attack-bound option (ATTB = 1) realizes a fast weak signal attack by limiting the detector ranges for recovery of the LEV and MPH detector to the range actually in use by weak signal processing. I.e. the LEV detector checks weak signal activity of softmute, or when HCMP = 0 of both softmute and high cut control, the MPH detector checks weak signal activity of stereo blend, or when HCMP = 1 of both high cut control and stereo blend. This way the detector is held at a setting near to the earliest weak signal activation, allowing the fastest reaction in case of bad signal conditions.

4.7.7 Weak signal processing in AM mode

High cut control and soft mute are also active in AM mode. The start values for high cut control and soft mute include settings for high levels to fit the AM requirements. All relevant settings are controlled by the same data bytes as in FM mode. The weak signal processing for AM is only controlled by the level voltage, the WAM and USN detectors are switched off and also the ATTB option is switched off.
During AM mode the read out of the level signal via I^2C is additionally filtered by the LEV detector to minimize the influence of AM modulation on the level measurement.

4.8 NICE tuning actions and control

The NICE TEA684xH tuners offer two tuning actions, AF update and Preset. Two control lines AFHOLD and AFSAMP control the TEF689xH muting and weak signal behaviour to support the tuning processes. The use of tuning actions and shared control reduces control complexity considerable.

4.8.1 Mute control of the TEF689xH

When the muting during an AF update or a Preset procedure is done in the TEF689xH, the bit AFUM in byte 4H (CONTROL) has to be set to 1. Both FM inputs FMMPX and MPXRDS of the TEF689xH are connected to the not muted output of the FM demodulator in the tuner. In NICE this is the output RDSMPX. This is the recommended application since the RDSMPX output of NICE realizes somewhat better noise performance. Also DC pops that may occur during manual tuning (due to off-grid reception) are suppressed when using Preset tuning with the recommended mute time.

When instead the tuner is used to provide the mute function the FMMPX input of the TEF689xH has to be connected to the mutable MPX output of the tuner (FMMPX of NICE) and the MPXRDS input has to be connected to the direct demodulator output (RDSMPX of NICE). The bit AFUM in byte 4H should be set to 0 to disable muting in the TEF689xH.

4.8.2 AF update

In the Radio Data System (RDS) a list of alternative frequencies for a program chain can be transmitted. When the received station is fading or is heavily distorted by multipath the radio can automatically tune to another station with the same program but better receiving conditions. To get the information about the signal quality of these alternative frequencies the radio should periodically tune to the alternative frequencies to check the signal quality. To the listener these quality checks should be inaudible. It is found that such checks are virtually inaudible when their overall duration is within 7 ms and the muting and demuting is done with soft slopes.

The NICE ICs provide an automatic process, the AF update sequence, which is started via I^2C bus. The NICE IC controls AF update support functions in the TEF689xH by two signal lines AFHOLD and AFSAMP. The AFHOLD signal is low during the whole AF update (usually 7 ms). When the tuning is finished the quality indicators of LEVEL, WAM and USN of the alternative station are evaluated at detectors in the TEF689xH. At the end of quality check this information is stored so the quality indicators can be read out at any later time by I^2C bus. After the information of the alternative station has been read, the detectors are reset and actual values of the received station are continuously present again.

The status of the content of the detectors is indicated by the bit AFUS in read byte 1. When first tuning is ready, the NICE sets the signal AFSAMP to HIGH. The AFSAMP signal sets the bit AFUS to 1. This indicates, that the quality information, which is now read out, is caused by the alternative station. After quality check has finished the tuner will tune back to the original frequency indicated by the AFSAMP signal going LOW. The AFUS bit however remains 1, until the stored quality information has been read out via I^2C bus. The function during the AF update is shown in Fig.18

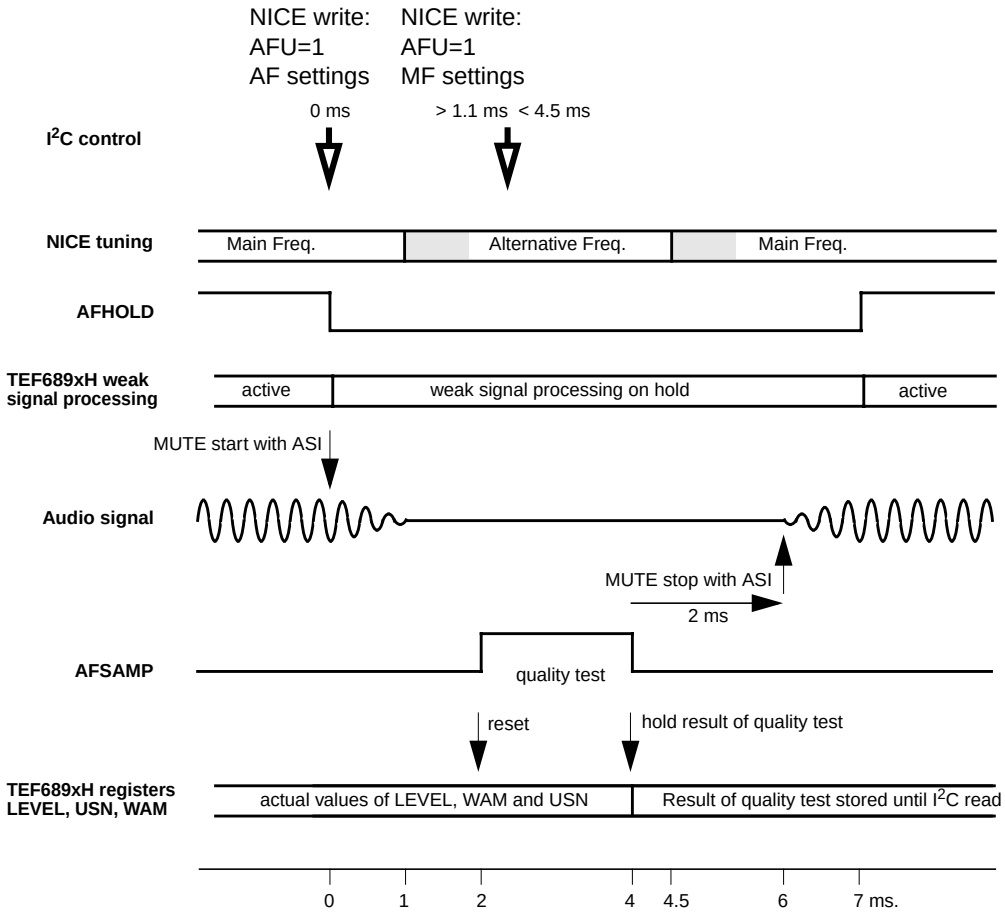


Fig.18 Timing of AF update procedure

At the beginning of the AF update AFHOLD is set to LOW by the tuner. If AFUM = 1 this starts the muting with ASI in the TEF689xH within the next 1 ms. The weak signal processing is stopped and the last values of the weak signal processing remain to be used during and to continue with after the AF update. The tuner is tuned to the alternative frequency, which takes about 1 ms. The end of tuning is indicated by AFSAMP = HIGH, at this

point the detectors for I^2C reading of USN and WAM are reset to assure final values within the 2 ms quality check. At the falling edge of the AFSAMP signal the values LEVEL, USN and WAM of the alternative station are stored. After the quality test these values are held, available for read out by the I^2C-bus. 2 ms after the HIGH to LOW transition of AFSAMP the demuting with ASI starts. The complete AF update is finished after 7 ms.

To avoid DC charging of the coupling capacitor between the tuner and the TEF689xH FMMPX input pin the input impedance is switched to high-impedance state during AF update (between 1 ms and 6 ms). This function avoids the occurrence of a DC offset pop in the audio signal when the alternative frequency station is not found but instead a neighbour channel is received. The FMMPX high-impedance switch is only active when muting is performed by the TEF689xH (AFUM = 1).

4.8.3 Preset tuning

For tuning to a new station the NICE tuner incorporates a second process; Preset. Also during Preset tuning some functions in the TEF689xH are controlled by the NICE. The AFHOLD signal is HIGH during the complete process as during normal operation. The start of the Preset tuning process is indicated by the rising edge of the AFSAMP signal. This sets the slow weak signal time constants of the LEV detector and the MPH detector to a fast time constant of 60 ms. When this Preset mute state is held for approx. 60 ms this enables the weak signal processing circuits to change ‘immediately’ to the new conditions which is a desirable function when changing station. The audio signal is muted with ASI within 1 ms. At the end of the Preset tuning the falling edge of the AFSAMP signal starts the demuting with ASI. The content of the registers LEVEL, WAM and USN follows continuously the actual values. No values are stored or held. See Fig.19

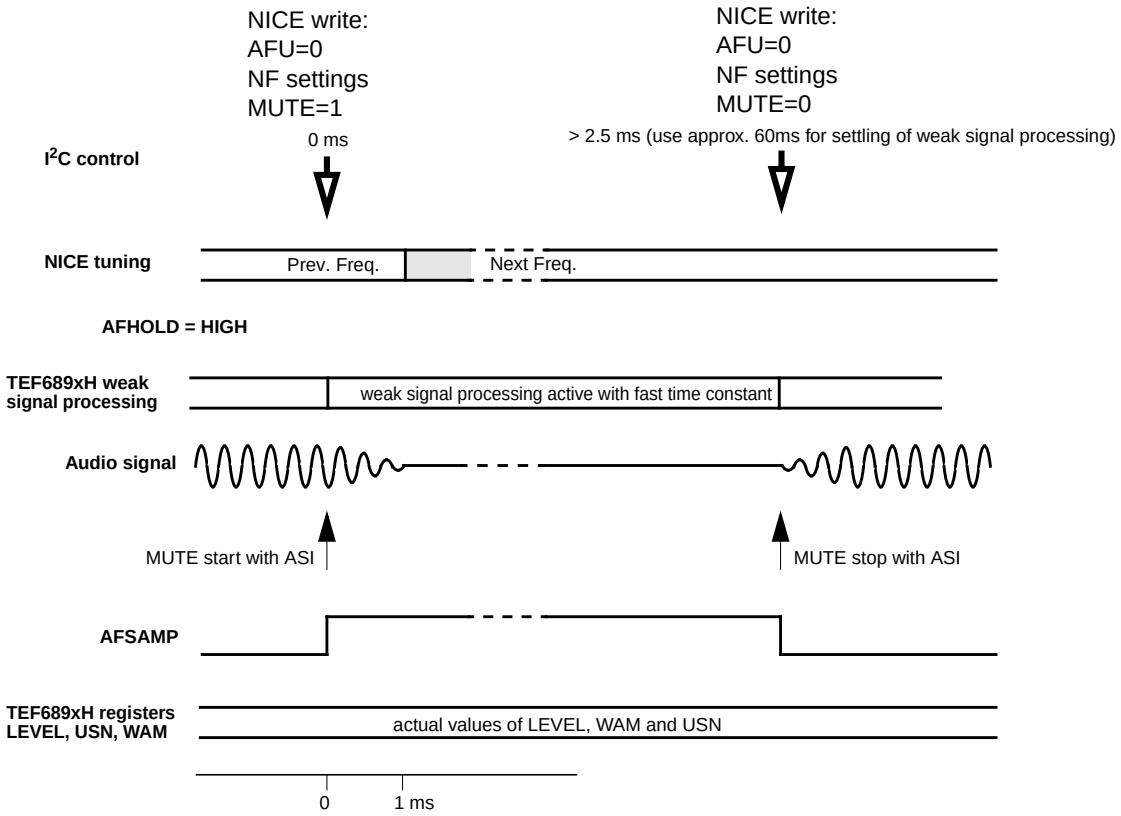


Fig.19 Timing of Preset tuning

4.8.4 I^2C tuning control of TEF689xH

Most of the tuning control that is automatically activated during NICE tuning via the AFHOLD and AFSAMP line can also be accessed via I^2C control.

Muting of the radio signal, as active during AF update and Preset, is possible by the RMUT bit.
Muting and demuting of radio mute is done via ASI with a fixed 1 ms time.

TABLE 17 Radio mute control, byte 4H

RMUT	RADIO MUTE
0	no mute (of radio signal)
1	mute (of radio signal)

Putting the weak signal processing on hold, as activated by AF update, is possible by the AFUH bit.
In case there is also control by the AFHOLD line (AFHOLD = LOW) AFUH will automatically reset to AFUH = 0.

TABLE 18 Weak signal processing hold, byte 4H

AFUH	WEAK SIGNAL
0	active
1	on hold

Changing the weak signal slow detector timings to fast, as activated by Preset, is possible by the SEAR bit.

TABLE 19 Weak signal processing fast, byte AH

SEAR	WEAK SIGNAL TIME
0	slow detector times
1	fast 60 ms detector time

4.8.5 Extended AF tuning

When by means of AF update checks an alternative frequency has been found with better signal conditions this frequency will be selected. However since frequencies are shared between stations that are located far away there always is a small chance that the received frequency is not really the desired alternative but instead a different station.
One way to go is to assume everything is OK and boldly change to the new frequency. In this case a standard Preset tuning can be used with a small delay time of at least 2.5 ms to mute the tuning process. The advantage of this approach is an inaudible switching in most situations however in case of a different program the produced error will be very observable.
A more safe approach is to mute until the program is found OK by checking the RDS PI (program identifier) code, the time needed for checking (up to 88 ms) will however cause the mute to be perceptible.
For this purpose Preset tuning can be used, however weak signal control will change fast to the new conditions which is undesired, this can be overcome however by activating weak signal hold via bit AFUH in byte 4H (CONTROL) and deactivating AFUH afterwards.
A more convenient way is using AF update tuning. When the second I^2C transmission is delayed the return tuning will be delayed beyond 4.5 ms and the following process will be delayed too. This way weak signal processing is held automatically. Also the inaudible mute of NICE is delayed this way, however when muting is performed in the TEF689xH this is not the case since the AFSAMP signal is not stretched. If muting is done in the TEF689xH the mute can be activated by use of the RMUT bit in byte 4H (CONTROL). See Fig.20

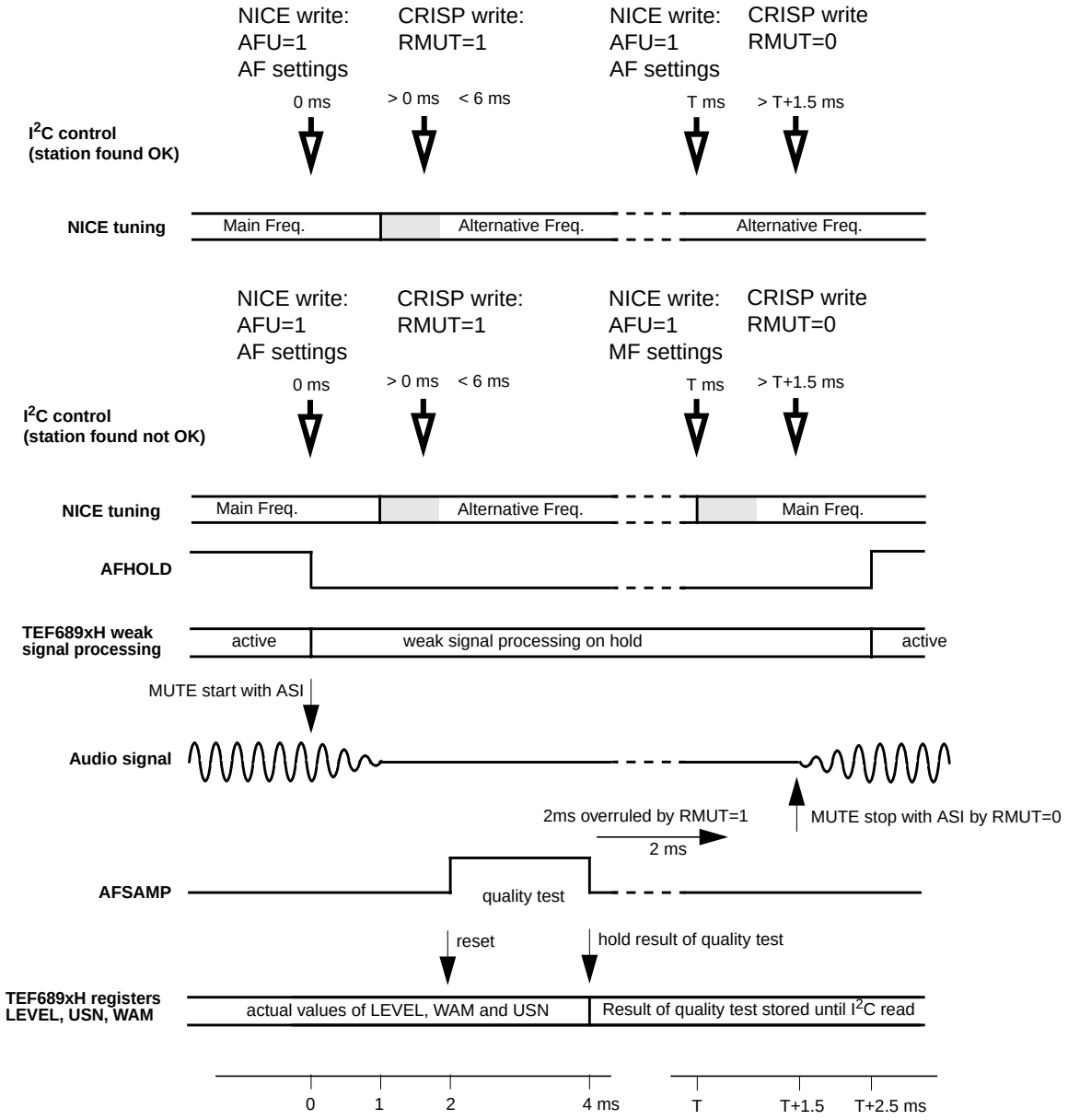


Fig.20 Timing of extended AF procedure using AF update tuning

4.9 Tone- and volume control

4.9.1 Input selector

The first block in this part is the input selector. The four input sources are selected by the bits INP1 and INP0 in byte BH as in Table 20.

TABLE 20 Input selector settings, byte BH

AUDIO SOURCE FOR TONE/VOLUME PART	INP1	INP0
Radio	0	0
CD	0	1
Tape	1	0
Phone	1	1

4.9.2 The ASI function

All tone/volume control blocks except the treble control use the audio step interpolation, ASI, to avoid the step noise during the audio control. The ASI function changes the desired setting in a smooth slope. With a longer duration of the ASI control the control step is less audible, but the process takes a longer time. Therefore the duration of this slope can be selected via I^2C bus in four steps (Table 21). The ASI function can also be switched off by bit ASI in byte BH: If ASI = 0, the audio step interpolation is disabled. With ASI = 1 it is enabled.

TABLE 21 Duration of the audio step interpolation ASI, byte BH

ASI TIME (ms)	AST1	AST0
1	0	0
3	0	1
10	1	0
30	1	1

The values in Table 21 are used for tone- and volume settings by the user of the radio. As described in the section weak signal processing, the ASI function is also used during the AF update and during the softmute in the weak signal processing. In these control functions different time constants are used.

4.9.2.1 AF update and Preset mute

During AF update and Preset the muting is done in the volume control part using the ASI function (AFUM =1). This realizes the necessary smooth muting and demuting to achieve an inaudible process. The AF update is always done with an ASI time constant of 1 ms. This is independent from the setting of the ASI time constants for the tone/volume control.

4.9.2.2 Softmute by weak signal processing

The softmute caused by the weak signal processing is also realized in the volume control part. The overall time duration, which is used for the soft mute is determined by the detectors in the weak signal processing and, of cause, also by the duration of the detected disturbances.
The ASI time constant for the muting by the weak signal processing, however, is always 1 ms. When a fast muting is required, as for instance from the USN part, the muting could be finished in 1 step within 1 ms. When

the muting has to follow a slow function as for instance caused by the level detector, the muting is done in a sequence of small steps of 1 ms each.

4.9.2.3 Multiple controls with ASI

During the operation of the radio ASI can be used by different, independent sources. The ASI can be started by a wanted control of the user, the weak signal processing, which depends on external influences, and the AF update or Preset, which is controlled by the main controller in the radio.

The step interpolation requires a specific pulse sequence, which controls the transition from one setting to another. This pulse sequence is generated by an ASI generator, which drives all controls with ASI.
The generator can control several ASI processes at the same time, but it can not start a new ASI control before the current process is finished.

4.9.2.3.1 ASI controls by the user.

Since the ASI generator can only control one transition at a time, the transitions need sequential processes. The ASI function starts immediately, when the byte is received, which contains new control information. When in one I^2C bus transmission loudness, volume and bass settings are changed, this is performed in two ASI processes. When the byte “loudness” has been received, the ASI control of loudness starts. The information about the settings in volume and bass are stored. When the ASI control of loudness is finished, the ASI controls of volume and bass are processed simultaneously. There is no delay between the two ASI controls.

A running ASI process will not be interrupted by sending new control information, even to the same control block. The running process will complete its cycle normally, immediately followed by a new ASI process to realize the latest setting. This is realized by three registers for ASI control data: start value, finish value and I^2C value.

When control of bass or fader includes a BASM or FADM mode change an intermediate setting of 0 dB is inserted automatically. In this case two ASI processes are generated for reaching the new bass or fader setting.

4.9.2.3.2 AF update or Preset during user controls

The ASI control of a tone/volume setting can be performed in a long period compared with the AF update or Preset mute. The tuning process could start when e.g. a bass setting with an ASI time of 30 ms is running. In the TEF689xH the tuning process has the priority. That means, that the bass control is interrupted, when the tuning process starts. This is necessary, because the AF update and Preset is controlled by the tuner and the tuner functions can not be delayed by the TEF689xH. Therefore the bass control is immediately set to its final value and the AF update is started at the same moment with its correct timing given by the NICE. Fig.21 shows the interruption of the ASI control of bass by an AF update.
If desired the controller can take care that an AF update is not started during a tone/volume control activity. It is possible to detect a running ASI control via I^2C bus. The bit ASIA (ASI active) indicates, that ASI is in progress. If ASIA = 0, ASI is not active. If ASIA = 1, an ASI control is in progress.

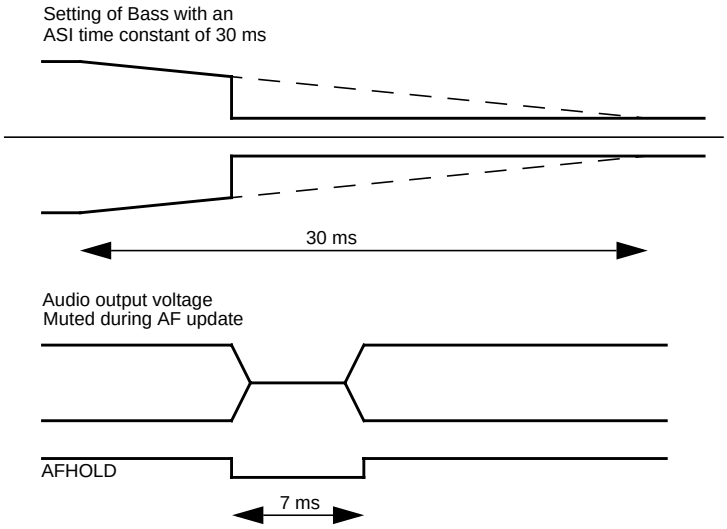


Fig.21 AF update during running ASI control of the tone/volume part

4.9.2.3.3 Weak signal processing control during user controls

It is possible, that the weak signal processing activates the soft mute or stereo blend while an ASI transition of the tone/volume part is in progress. In this case the running ASI process is finished, but with an increased ASI speed. The ASI generator is set to its shortest ASI time 1 ms. With this timing the process is continued. The function is explained in Fig.22. A bass setting with an ASI time constant of 30 ms is in progress. After 9 ms the weak signal processing activates the soft mute. At this time 30% of the bass transition is finished. The remaining 70% are now done with the fastest ASI timing constant of 1 ms. This takes another 0.7 ms to close the bass setting. Now the soft mute starts according to the requirements of the weak signal processing.

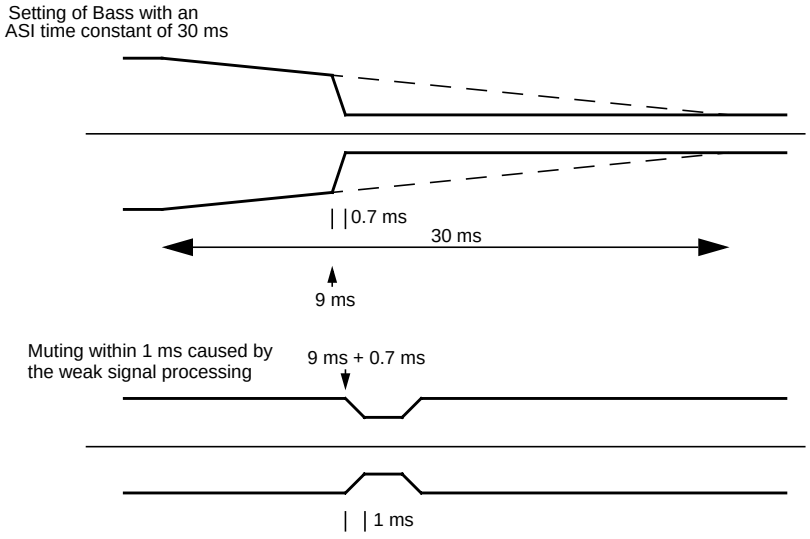


Fig.22 Soft mute caused by the weak signal processing during user controls

4.9.2.3.4 AF update during ASI control by the weak signal processing

A soft mute or stereo blend process could be started by the weak signal processing just before the beginning of an AF update. In this case the ASI process by the weak signal processing would be interrupted by the AF update and completed without any ASI. (see Fig.21) In theory this may produce audible steps however this has never been found in practice. If it is desired to avoid step noise also in this case, AF update can be prepared by deactivating the weak signal processing influence. Setting AFUH to 1 sets the weak signal processing on hold independently from the AFHOLD control line. When this is done before the tuning starts, the tuning process can not interrupt a running ASI control. AFUH is reset to 0, when the AFHOLD input is LOW. Thus for AF update it is not necessary to set AFUH to 0 via I^2C bus.

4.9.3 Loudness

The loudness section provides a gradual transition from a linear frequency response to a response with bass boost only or bass and treble boost. This compensates the characteristic of the human ear when the user varies the volume setting. The attenuation of the loudness block can be varied from 0 dB to - 20 dB at 1 kHz with a step size of 1 dB and should be used as part of the volume control range. The loudness filter function can be disabled effectively by using loudness for the ‘volume’ steps below the actual volume range. The loudness attenuation is controlled by bits LDN4 to LDN0 in byte CH.

The bass boost response is always used. The bass frequency can be set to 50 Hz or 100 Hz by bit LLF in byte CH. The bass frequency is that frequency at which the attenuation of the lowest setting (-20 dB) is 3 dB. It is possible to disable the boost of high frequency components. Bit LHB in byte CH controls high boost.

The four possible frequency response curves are displayed in Fig.23 to Fig.26

LLF	LHB
0	1

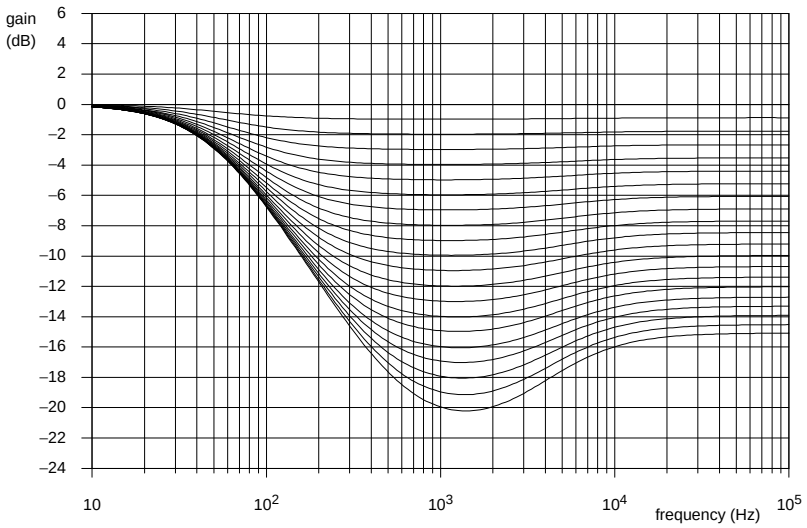


Fig.23 Loudness control, bass boost frequency 50 Hz, high boost on

LLF	LHB
0	0

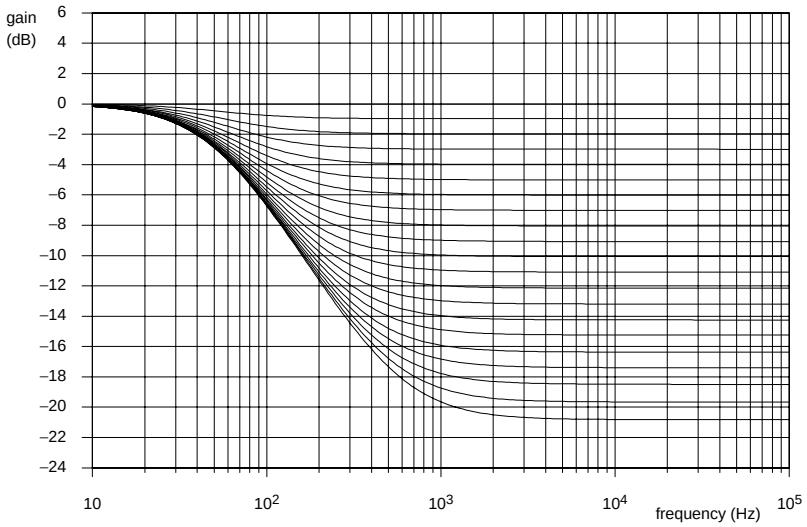


Fig.24 Loudness control, bass boost frequency 50 Hz, high boost off

LLF	LHB
1	1

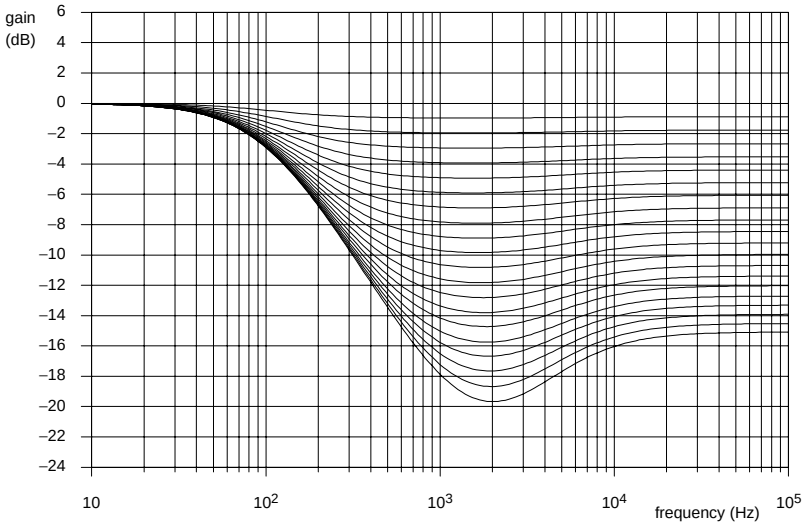


Fig.25 Loudness control, bass boost frequency 100 Hz, high boost on

LLF	LHB
1	0

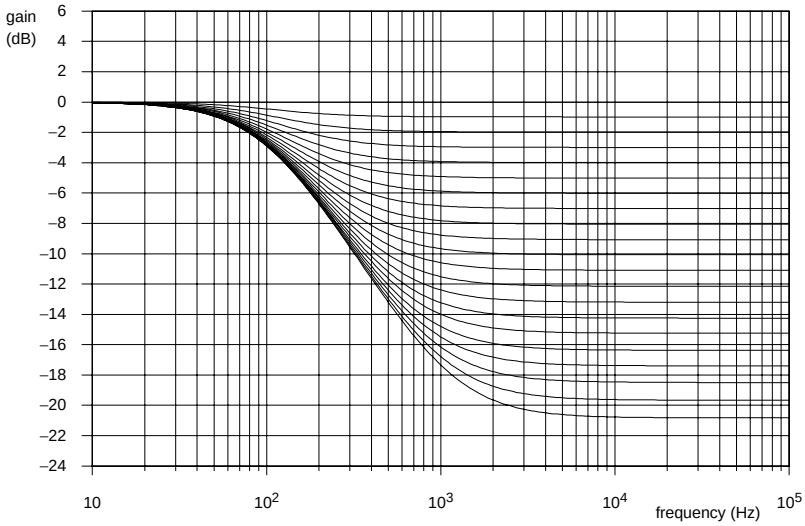


Fig.26 Loudness control, bass boost frequency 100 Hz, high boost on

4.9.4 Volume and balance control

The volume control block is used for volume setting, balance control and muting of the audio signal. The gain or attenuation of this block is controlled by I^2C-bus for the volume setting by the user of the radio.

The mute function of this block is used in the AF update and Preset process for muting with 1ms ASI slopes. This special radio mute can also be activated by bit RMUT in byte 4H, the radio signal is muted with RMUT = 1. General muting can be activated by the bit MUTE in byte BH. The audio signal is muted with MUTE = 1. The variable attenuation is used by the weak signal processing for the soft mute. The radio mute and the soft mute are controlled by internal circuits. They can not be influenced by the control of the volume part.

The volume control can be set from a gain of 20 dB to an attenuation of 59 dB. Together with the loudness part the overall attenuation range is 79 dB. The last setting of the volume control is muting with a mute attenuation of >80 dB. The volume part is controlled by bits VOL6 to VOL0 in byte DH.

The volume control part is also used to adjust the balance of the left and right stereo channel. One channel is attenuated compared with the other one in steps of 1 dB to a maximum attenuation of 79 dB. If balance attenuation exceeds the volume control range the channel is muted. The ratio of the attenuation is selected by bits BAL6 to BAL0 in byte 11H. The bit BALM determines, which channel is attenuated. With BALM = 0 the left channel is attenuated and with BALM = 1 the right channel is attenuated.

4.9.5 Combined volume control using Volume and Loudness

For control flexibility to the car-radio manufacturer loudness and volume use separate controls, this way different ‘loudness’ functions can be realized. The micro-controller software has to realize combined control in such a way that a single ‘volume’ control with ‘loudness’ function is available to the end user. One commonly used control algorithm is shown below.

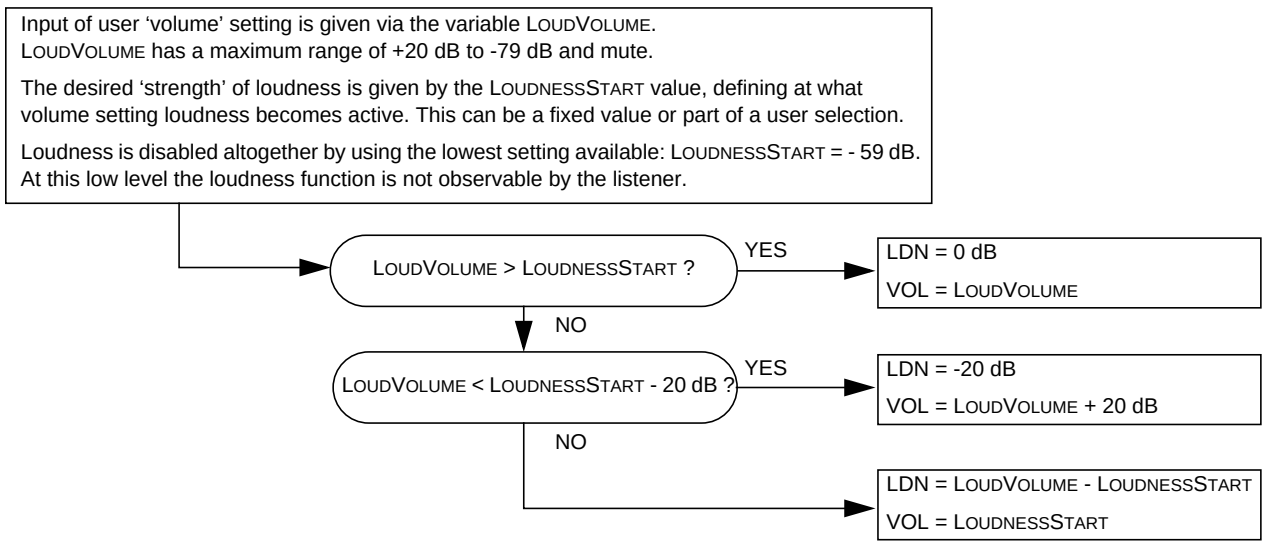


Fig.27 Program control flow for Loudness and Volume

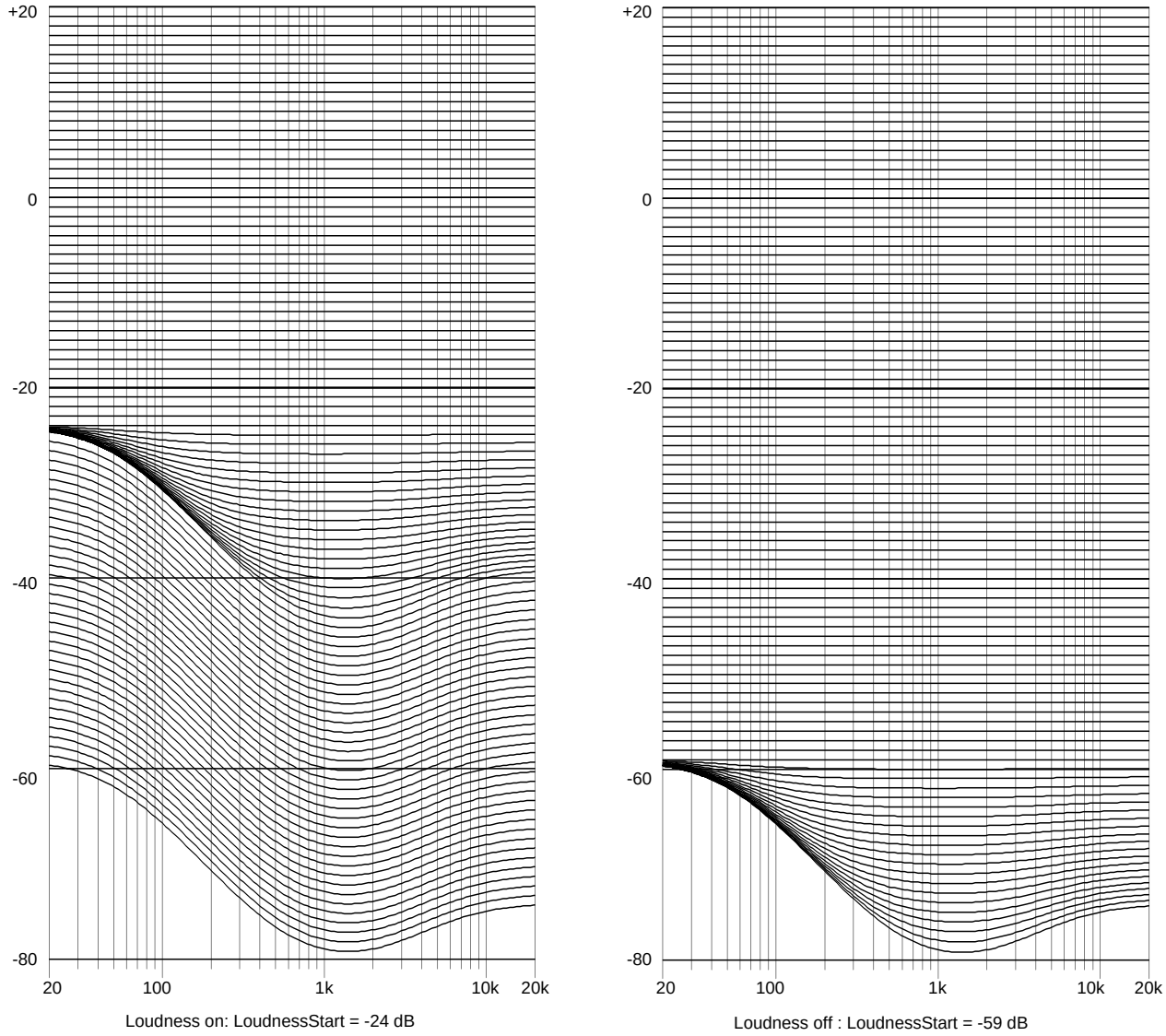


Fig.28 Example of volume with loudness control and loudness off

Note: when Loudness on/off or selection of LoudnessStart is part of the user control the I^2C transmission for changing from higher to lower LoudnessStart values (e.g. from -24 dB to -59 dB) is best created by two transmissions changing Volume first. This to avoid a momentary increase of overall volume between the ASI control of Loudness and Volume.

4.9.6 Treble control

The treble block controls the gain or attenuation of the high frequency components. The treble frequency can be set to four different values by bits TRF1 and TRF0 in byte EH. see Table 22. The treble frequency is the frequency at which the selected gain or attenuation is achieved.

TABLE 22 Setting of the treble frequency, byte EH

TREBLE FREQUENCY (kHz)	TRF1	TRF0
8	0	0
10	0	1
12	1	0
15	1	1

TRF1	TRF0
0	0

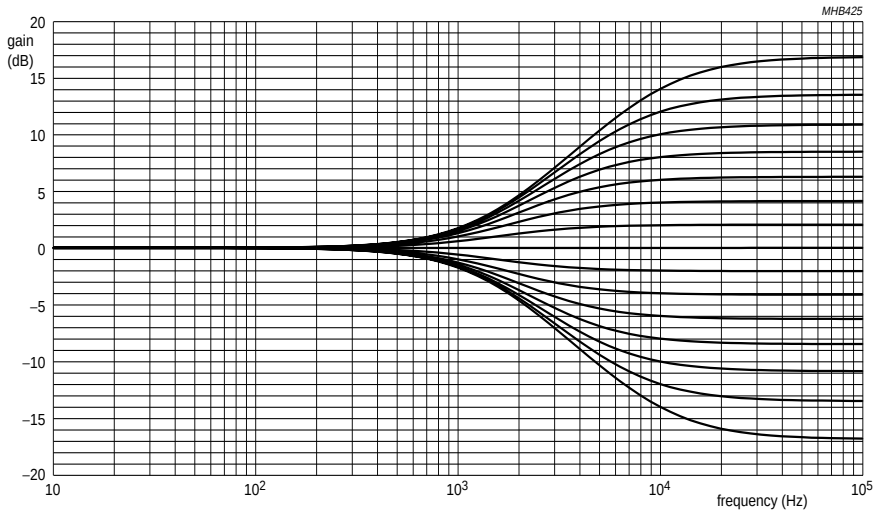


Fig.29 Treble control, treble frequency 10 kHz

A set of typical curves with a treble frequency is shown in Fig.29. The value of treble gain or attenuation is set by bits TRE2 to TRE0 in byte EH in 2 dB steps from 0 to 14 dB. The treble mode bit TREM in byte EH selects gain or attenuation. TREM = 0 sets the treble mode to attenuation and TREM = 1 sets it to gain.

4.9.7 Bass control

In the bass control four different bass frequencies can be selected by bits BAF1 and BAF0 in byte FH. The bass frequency is the centre frequency of the bass bandpass response.

TABLE 23 Setting of the bass frequency, byte FH

BASS FREQUENCY (Hz)	BAF1	BAF0
60	0	0
80	0	1
100	1	0
120	1	1

The characteristic of the bass response is set with bit BASH in byte FH. BASH = 0 sets the bass response to a band-pass response. With BASH = 1 the bass response is a shelve curve. The shelve curve is only guaranteed for bass attenuation (BASM = 0). Fig.30 and Fig.31 show typical frequency response curves of the bass control.

The value of bass gain or attenuation is set by bits BAS2 to BAS0 in byte FH in 2 dB steps from 0 to 14 dB. The bass mode bit BASM in byte FH selects gain or attenuation. BASM = 0 sets the bass mode to attenuation and BASM = 1 sets it to gain.

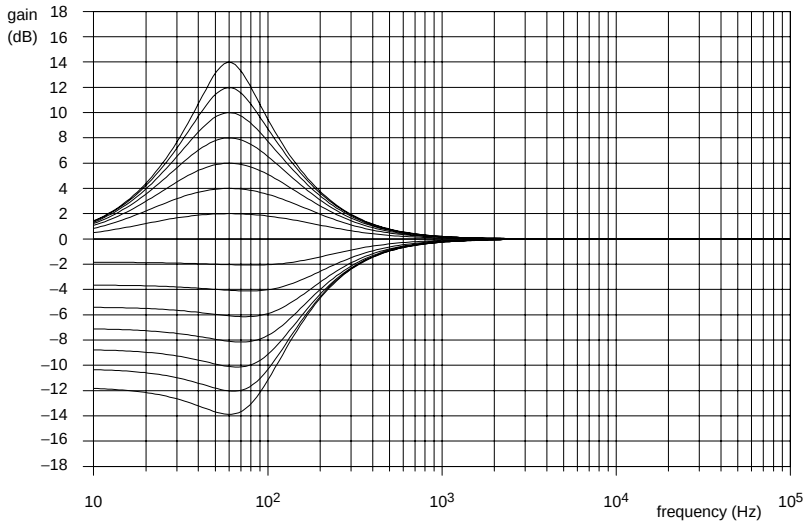


Fig.30 Bass amplitude control, bass frequency 60 Hz, band-pass boost, shelve cut

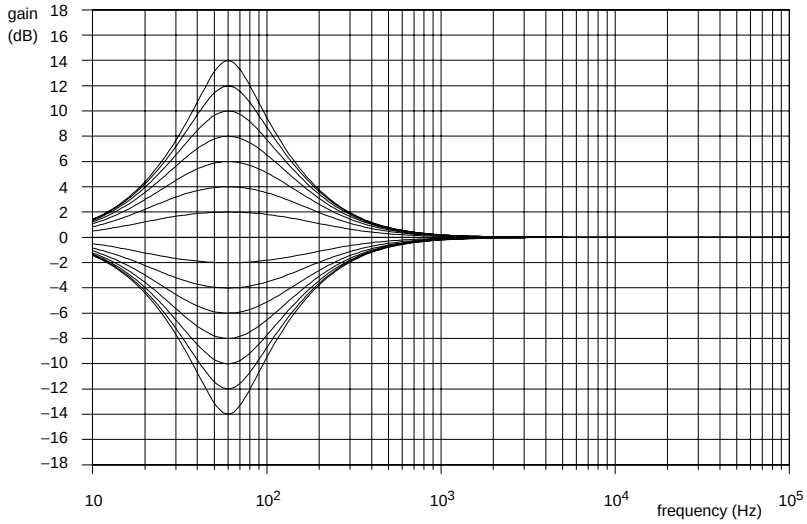


Fig.31 Bass amplitude control, bass frequency 60 Hz, band-pass boost, band-pass cut

4.9.8 Fader

The fader controls the attenuation of the front or rear channels separately. One pair of channels is attenuated, the other passes the circuit directly. Bit FADM in byte 10H selects the attenuated channels. If FADM = 0, the front outputs are attenuated. The rear output is attenuated when FADM = 1.

The range of attenuation is from 0 to 59 dB.
The setting of the attenuation is done with bits FAD4 to FAD0 in byte 10 H.
The step size is 1 dB for α = 0 dB to α = 15 dB (16 steps)
2.5 dB for α = 15 dB to α = 45 dB (12 steps)
3 dB for 45 dB to 51 dB
4 dB for 51 dB to 59 dB.
With these step sizes it is possible to cover the whole range of 59 dB with 5 bits.

The fader circuit allows the muting with ASI of each output channel separately. This is used to apply additional signals as beep or navigation voice signals to the outputs instead of the audio signals. The mute function is controlled by bits 3 to 0 in data byte 12H, the ASI time constant is the same as in the other circuits of the tone/ volume part. (Table 21)

TABLE 24 Muting of the audio channels in the fader part, byte 12H

BIT	AUDIO CHANNEL	0	1
MULF	left front	audio signal on	audio signal muted
MURF	right front		
MULR	left rear		
MURR	right rear		

4.9.9 Output mixer

The output mixer selects the audio signal at the four audio output pins LF (left front), RF (right front), LR (left rear) and RR (right rear).

The signal from the beep generator, the external source connected to the NAV-input, or the combination of both can be applied to each output separately. Together with the mute function in the fader this allows to add the additional signal to any channel or to replace the audio signal by the additional signal. The beep generator can be switched off by selecting mute with the beep level setting. The NAV input is enabled by bit NAV in byte 12H. With NAV = 0, the NAV input signal is muted, NAV = 1 enables the NAV signal.

The mixer is controlled by the data byte 12H as shown in Table 25

TABLE 25 Mixing of beep or NAV signals to the audio signals, byte 12H

BIT	AUDIO CHANNEL	0	1
MILF	left front	no beep and NAV	beep or NAV mixed to audio signal
MIRF	right front		
MILR	left rear		
MIRR	right rear		

4.9.10 Beep generator

The beep generator generates an audio signal for warning and indication purposes. The beep signal is a sine wave signal with adjustable output level and frequency. The level is selected with bits BEL2 to BEL0 in byte 13H and the frequency is set by bits BEF1 and BEF0 in byte 13H according to Table 26 and Table 27

TABLE 26 Setting of the beep level, byte 13H

BEEP LEVEL (mV)	BEL2	BEL1	BEL0
mute	0	0	0
13	0	0	1
18	0	1	0
28	0	1	1
44	1	0	0
60	1	0	1
90	1	1	0
150	1	1	1

TABLE 27 Setting of the beep frequency, byte 13H

BEEP FREQUENCY (Hz)	BEF1	BEF0
500	0	0
1000	0	1
2000	1	0
3000	1	1

Switching the beep signal via the beep level or output mixer control does not use the ASI function. Instead the beep signal is started at a positive zero crossing and switching actions are delayed until the next positive zero crossing to avoid modulation clicks.

4.10 Test modes

Several test modes are implemented for evaluation and IC production test purposes. These test modes are selected by bits TST in data byte 2H. Test modes may use some of the ‘unused’ pins or change a standard pin function. For application use the test modes should be left disabled by selection of test 0.

TABLE 28 Test modes, byte 2H

TEST	FUNCTION	TST3	TST2	TST1	TST0
Test 0; No test	standard application	0	0	0	0
Test 1 to test 31	test modes	x	x	x	x

5. RDS

RDS (Radio Data System) and RBDS (Radio Broadcast Data System) are standards for transmitting digital information over conventional FM transmitters. Data generally consists of program-related information like station name and program name as well as general information like e.g. traffic messages. Also a list of alternative frequencies for transmitters carrying the same program can be part of the data.

The combination of the TEF689xH with a NICE tuner (TEA684xH) fully supports background quality checks of such AF (alternative frequency) signals and switching to the best signal conditions without audible artifacts by means of the AF update function. In many countries RDS has become a standard feature for car-radio receivers.

5.1 RDS demodulator

The TEF6890H/TEF6892H offers a fully integrated RDS/RBDS demodulator function. Clock, Data and Quality output signals are available for connection to a decoder for decoding of the RDS data stream. In case of the TEF6890H the decoder function has to be realized in the micro controller software, in case of the TEF6892H the decoder is integrated and the decoded RDS data is available via I^2C.

RDS and RBDS differ in data structure but use the same modulation scheme and can therefore use the same demodulator. Because the RDS function uses the integrated PLL no external crystal is required. For R(B)DS the PLL has two functional modes; reference PLL and pilot PLL mode. In case of reception of an FM-stereo signal the PLL locks to the 19 kHz stereo pilot signal for use with both the stereo decoder and the RDS demodulator. Because the pilot frequency has a fixed relation to the 57 kHz RDS carrier this sets the optimum condition for RDS / RBDS reception. In case of a mono transmission with RDS the PLL changes to reference PLL mode, locking to the reference frequency delivered by the NICE tuner. The reference PLL system itself only introduces an error of 1 ppm so frequency accuracy is fully defined by the 20.5 MHz NICE crystal. The crystal accuracy requirements for a tuner application guarantee good RDS / RBDS reception at the same time.

RDS reception remains available also during AM mode or selection of a different audio source as long as a valid tuner signal is present at the MPXRDS input pin. If the RDS functionality is not required it can be disabled altogether using the RDS-stand-by option (STBR = 1).

Two demodulator output modes are available via I^2C control; direct output mode and buffered output mode. Direct output mode (CLKO = 1, CLKI = 0) is compatible with stand-alone demodulators like the SAA6579T and SAA6581T. Buffered output mode (CLKO = 0, CLKI = 1) includes a 16 bit data buffering for reduced micro controller load and is compatible with the buffered mode of CDSP devices like the SAA7705H.

TABLE 29 Demodulator output mode control, byte 2H

DEMODULATOR OUTPUT MODE	CLKO	CLKI
reserved	0	0
16 bit buffered output mode	0	1
direct output mode	1	0
reserved	1	1

Note: For the TEF6892H these bits also control some decoder output functionality (see Table 34).

For direct output mode output signals of clock (RDCL), data (RDDA) and quality (RDQ) are available at a rate of 1187.5 Hz (842 μs) synchronized to the incoming RDS / RBDS signal data rate. Data and quality can be read at either the positive or negative going clock edge. Data and quality will change 4 μs before a clock edge, depending upon the lock condition this can be at the positive or negative going clock edge. Independent of lock condition and selected clock edge data and quality will remain valid for at least 400 μs. During poor reception it is

possible that faults in phase occur, the clock signal will stay uninterrupted but data and quality may shift by plus or minus 0.5 clock period (bit slip). The demodulator signal condition is evaluated for each received data bit and a good data (RDQ = 1) or bad data (RDQ = 0) quality judgment is available together with the data bit.

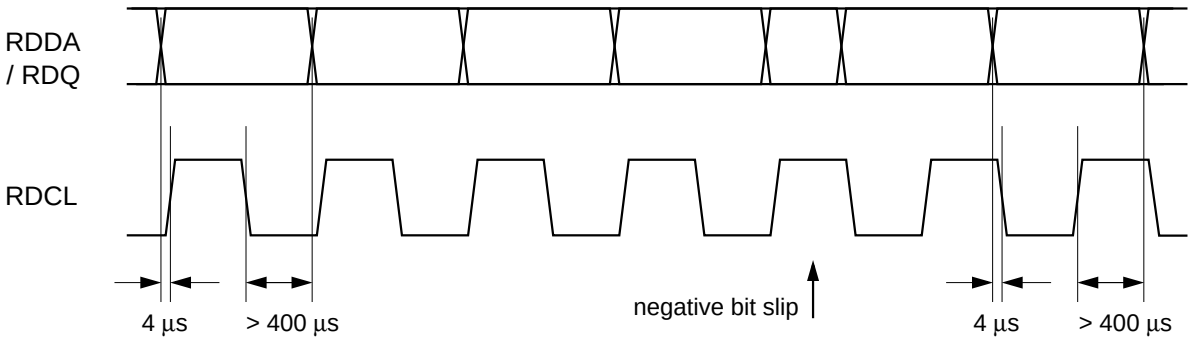


Fig.32 RDS timing in direct output mode.

Buffered output mode activates a dual 16 bit data buffer. While one buffer is written by the internal clock signal the other can be read out by a clock signal at pin RDCL, now used as input. Buffer full is signalled by the RDDA data / data-available line going low. When this condition is detected data can be read out by the micro controller clock with data changing at the clock high to low transition. After 16 positive clock pulses data reading is completed and the data line will remain high, transmission is ended by taking the clock high. Data available should be checked by the micro controller at least every 13.4 ms including the time needed for buffer read. Quality information is not part of the buffered information but remains active as in direct output mode.

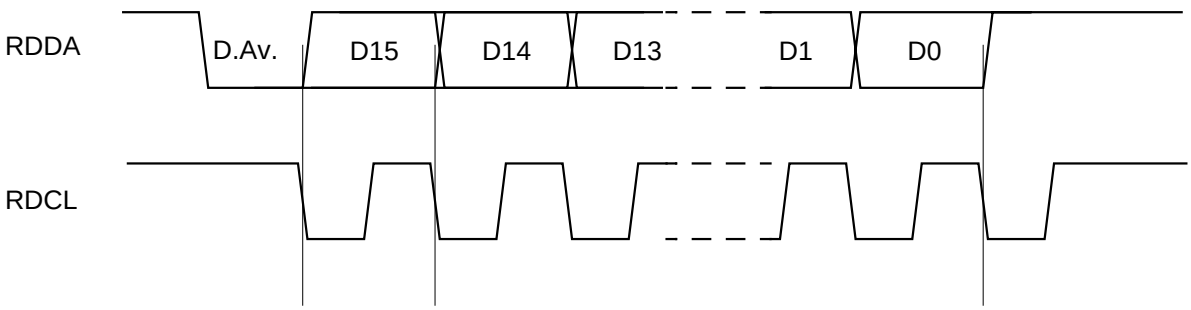


Fig.33 RDS timing in buffered output mode.

5.2 RDS decoder

For easy implementation of the RDS function an RDS / RBDS decoder is included in the TEF6892H. At the transmitter the original RDS / RBDS block data of 16 information bits are encoded by means of a so called ‘shortened cyclic code’ upon which a block identification code is added, realizing a total of 26 bits per block on the RDS data stream. The encoding allows for identification of the block start, detection of timing errors (bit slip) and detection and correction of bit errors introduced by poor reception. The RDS decoder performs the task of translating the encoded RDS data stream back to the original RDS information bits by means of syndrome detection, block synchronization, error correction and flywheel function.

Different decoder operation modes can be selected to fit the requested application use. The I^2C bit arrangement of the decoder of the TEF6892H is compatible with the CDSP SAA7709H and function and control are backwards compatible with both the SAA7709H and the stand-alone processor SAA6588.
Depending upon the selected mode the reception of one or two new blocks is signalled to the micro controller, either by means of read bit RDAV (read byte 1) or output pin RDDA. Up to two blocks of RDS or RBDS data and status information are available to read out via the I^2C-bus.

RBDS is a later extension to the RDS system for use in the United States. RDS and RBDS use the same modulation and data encoding however for RBDS an additional block type is defined. In case of RDS the data blocks are transmitted in groups consisting of an A, B, C (or C’) and D block, in case of RBDS however such a group can also consist of four E blocks. The E block data, referred to as ‘MBS’ or ‘MMBS’, is used for specialized functions like radio paging, emergency warning or broadcaster in-house use. Generally the MMBS information is not of interest to the radio user, however the decoder has to allow for E blocks since these would otherwise be interpreted as invalid blocks caused by reception errors. Bit RBDS realizes the selection of RDS or RBDS decoder mode, the valid or invalid use of E blocks influences both synchronization search and the detection of synchronization loss by the flywheel function (see “5.2.4 Synchronization flywheel”).

TABLE 30 RDS / RBDS mode, byte 1H

SYSTEM MODE	RBDS
RDS mode	0
RBDS mode	1

5.2.1 Synchronization search

At the start of RDS reception the decoder will decode the RDS stream by means of ‘syndrome calculation’ to look for block identification. Since specific data patterns or reception errors may also lead to block identification a more complex synchronization scheme is required for reliable synchronization. After a first block has been identified the decoder will look for occurrence of a second block with an expected code and expected position based on the first block and the block order allowed for an RDS or RBDS stream. When this second block has been found the decoder is synchronized and will start output of the decoded RDS data starting with the two blocks that lead to synchronization. The status of synchronization is signalled by means of read bit SYNC in read byte 4. SYNC = 0 signals synchronization search, SYNC = 1 signals synchronization found.

The synchronization process can be influenced by several settings, the most obvious is the already mentioned selection of RDS or RBDS mode via bit RBDS (byte 1H, RDS SET B).

During synchronization search for RDS mode blocks out of a block sequences of A - B - C (or C’) - D - A -... are searched for, however in case of RBDS mode also a sequence of E - A and D - E is allowed. The block sequence of E - E is not used for synchronization search because the E block identification code of ‘0’ is susceptible to synchronization errors. Synchronization will be established also when in the wrong mode but the appropriate mode setting will realize more reliable synchronization in case of RDS and faster synchronization in case of RBDS. After synchronization the presence of E blocks can be checked to find what type of RDS is received.

Note: some radio stations use RBDS with very long sequences of E block groups or skip the standard RDS group altogether. In this case synchronization will be delayed or not be found at all. Should MMBS reception be required for these situations synchronization search on E - E block sequences can be activated by means of a special MMBS mode selection of BIT 6 = 1 in byte 2H (RDS CLK). At this time the TEF6892H MMBS function is not public and only guaranteed ‘as is’.

When for synchronization search the first error free block has been identified the search for the second expected block can include error correction if desired. During poor reception conditions the use of error correction will improve the chance of finding synchronization. The use of error correction can be selected by bits SYM.

TABLE 31 Setting of error correction use, byte 0H

BLOCK VALID JUDGMENT	SYM1	SYM0
only error free blocks	0	0
up to 2 corrected bit errors	0	1
up to 5 corrected bit errors	1	0
only error free blocks (up to 5 corrected bits when synchronized)	1	1

The SYM setting is also active when synchronized and then influences the flywheel control. Note that there is no control over the error correction itself, SYM only controls the judgment of valid (good) or invalid (bad) blocks.

To further increase synchronization speed at poor reception it is possible to allow one or more blocks to be invalid between detection of the first block and the second block. This is controlled by bits BBG (bad block gain).

TABLE 32 Setting of bad blocks allowed during synchronization, byte 4H

BAD BLOCKS USE	BBG4, 3, 2, 1, 0
two way synchronization, no invalid blocks allowed	0 (00000B)
one way synchronization, BBG defines number of invalid blocks allowed	1 - 31 (00001B - 11111B)

It should be noted that increasing the speed of synchronization by allowing error correction or bad blocks also increases the chance of false synchronization on noise signals. Furthermore in case of a setting of BBG = 0 a more effective synchronization method is enabled where two synchronization attempts can be run in parallel (two way synchronization search), this can improve synchronization speed especially for good signal conditions.

When synchronized the flywheel function will automatically start a new synchronization when needed. However when tuning to a new station it can be desired to start a new synchronization ‘by hand’. Setting of NWSY = 1 will start a new synchronization, NWSY resets automatically so it is not necessary to set NWSY = 0 by I^2C.

TABLE 33 new synchronization start, byte 3H

SYSTEM MODE	NWSY
normal operation	0
new synchronization start	1

The synchronization search process can be followed by reading the I^2C block data but normally this is not of real interest and there is no signalling of data available via I^2C or pin. However to support the fastest finding of PI (program identifier) code it is possible to signal reception of an A or C’ block during synchronization search via bits DAC = 01B, byte 3H (fast PI search mode).

5.2.2 Data available signal

Different output modes can be selected for the signalling of data available via bits CLKO, CLKI and DAC.

TABLE 34 Decoder output mode control, byte 2H

DECODER OUTPUT MODE	CLKO	CLKI
data available at pin RDDA	0	0
reserved	0	1
data available or continuous rate at pin RDCL	1	0
reserved	1	1

TABLE 35 Data available control, byte 3H

DATA AVAILABLE SIGNAL	DAC1	DAC0
standard mode	0	0
fast PI search mode	0	1
reduced data request mode	1	0
decoder bypass mode	1	1

The availability of new block data can be detected via I^2C by checking the value of bit RDAV in read byte 1, RDAV =1 signals data available. Alternatively the voltage at pin RDDA or RDCL can be used, output LOW signals data available. The signalling via bit RDAV is available for all operational modes, the pin use however differs between modes.

A setting of DAC = 11B activates decoder bypass mode and disables the data available pin outputs altogether, instead pin RDDA and pin RDCL can be used equal to the TEF6890H for direct demodulator output or buffered demodulator output depending upon the setting of CLKO, CLKI (see “5.1 RDS demodulator”). The decoder however remains active during decoder bypass mode and data available is signalled by bit RDAV equal to DAC standard mode.

For the three DAC mode settings other than decoder bypass mode the RDDA or RDCL pin can be used for data available signalling. Checking the pin voltage or use of the pin signal to generate a micro controller interrupt can be used to realize a faster detection by the micro controller then possible by I^2C.
Pin RDDA is going LOW at the moment that new block data is available, this is the standard data available pin signal. When data is being read by the micro controller the signal will reset to HIGH. Instead of bit RDAV which is reset when the actual RDS block data has been read the pin signal will already reset after the first read byte. The pin signal will also reset to HIGH after a fixed time of 10 ms to allow direct connection to a micro controller with positive edge interrupt detection.

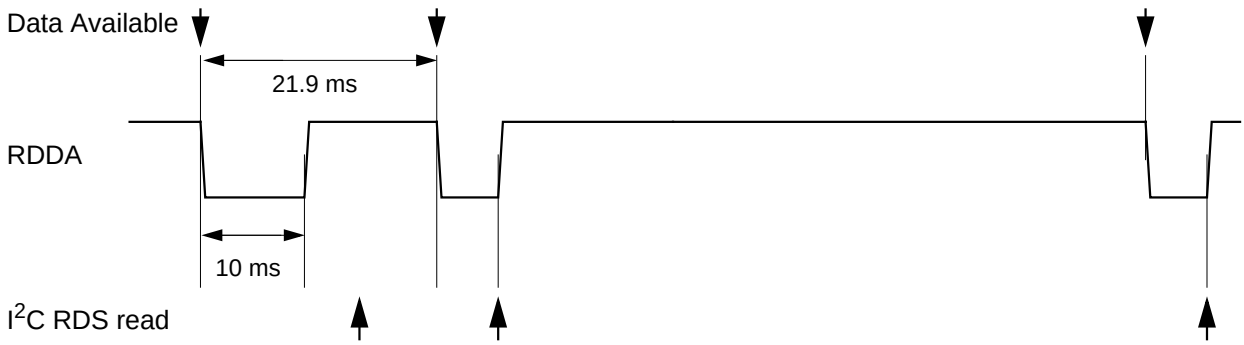


Fig.34 Data available timing at pin RDDA.

For micro controller timing purposes it may be desired to have a signal output at the RDS block rate of 21.9 ms, also when no RDS is received. For this purpose a setting of CLKO = 1, CLKI = 0 will activate pin RDCL to deliver a continuous block rate signal. In case of RDS reception the pin RDCL signal equals pin RDDA but when no RDS is received pin RDCL will continue to deliver LOW pulses at an internally generated fixed 21.9 ms rate. When the synchronization status changes no accurate timing can be realized however, at synchronization loss RDCL timing will be up to 23.6 ms for one period and when synchronization is found again after a short time the RDCL timing may be down to 20.2 ms as shown in Fig.35. When changing stations or when synchronization was lost for a long time the RDCL signal timing may deviate between 1.6 ms and 21.9 ms for one or two periods, depending upon signal phase the first HIGH to LOW transition indicating data available may be delayed by less than 1 ms.

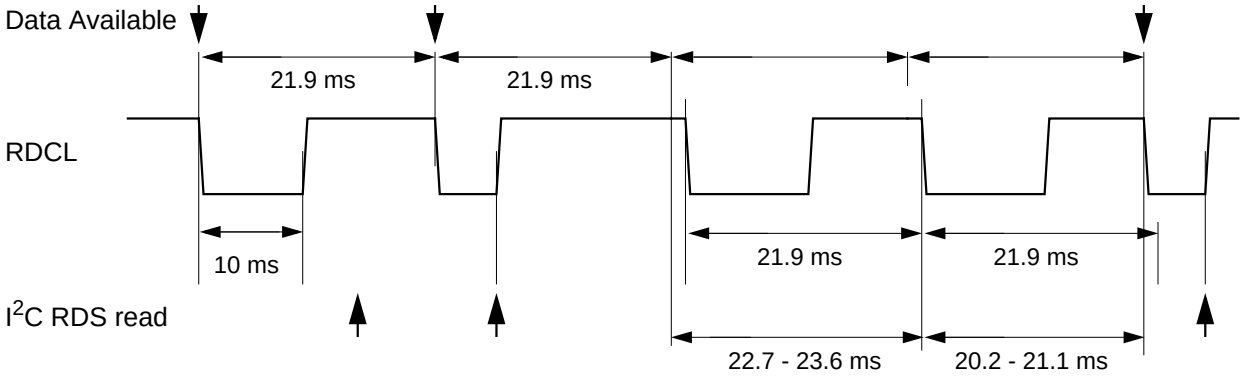


Fig.35 Data available timing at pin RDCL (CLKO = 1, CLKI = 0).

The DAC setting of 00B activates standard mode. In this mode data available is signalled at every new received block when synchronized. This mode assumes data is being read at every block and when this is the case, i.e. the data is read within 21.9 ms after data available, the single block data is always found in the ‘LAST’ data memory and the content of the ‘PREVIOUS’ data memory can be ignored.
Should the data reading occur after 21.9 ms a data overflow is signalled by bit DOFL = 1 (read byte 4), this indicates that instead of one, two blocks are present with the first block available as ‘PREVIOUS’ and the second block as ‘LAST’ information. In case of using two blocks the data reading should be finished within 42 ms after the first data available, otherwise newer blocks can not be handled any more and the newer data will be lost.

A DAC setting of 01B, fast PI search mode, equals standard mode when synchronized. However when during synchronization search an A block or C’ block is identified this will also be signalled as data available but bit SYNC reads 0 (read byte 4H) to indicate synchronization search. An A block and the sometimes used C’ block contain the program identifier (PI) code of the transmitter. This information can be used to judge if a received signal is indeed the intended radio program, especially of use when changing to an alternative frequency. Fast PI search mode signals the first occurrence of a PI code already during synchronization search realizing the fastest PI check possible. Although the other modes never signal data available during synchronization search the detected blocks can be read via I^2C, in case of fast PI search this data is restricted to A and C’ blocks only.

The DAC setting of 10B activates reduced data request mode. This setting equals standard mode but data available is signalled at every two new received blocks when synchronized. This mode assumes data is being read two blocks at a time so data overflow is only signalled (DOFL = 1) when RDS data is actually lost, i.e. when data is not read within the 42 ms time frame.

In any DAC mode the first data available with synchronization found status (SYNC = 1) is signalled at the moment that synchronization is found, i.e. at detection of the second expected block. The RDS data delivered via I^2C contains the two blocks that were used for synchronization with the first block in the 'PREVIOUS' register and the second block in the 'LAST' register.

5.2.3 Status information and block data

As already indicated the TEF6892H has a memory capacity of two RDS data blocks.
The last received RDS block data (LM) can be read via read byte 5 and read byte 6; RDS LDATM / LDATL.
The previous received RDS block data (PM) can be read via read byte 7 and read byte 8; RDS PDATM / PDATL.
Like all I^2C information the RDS data bits are ordered msb first.

Next to the RDS data the block identification code and the error status are given. Note that the delivered data and status information does not discriminate between good and bad blocks or block type, as long as the RDS decoder remains synchronized any received data is signalled as data available and the decoded information and data can be read by I^2C. Ignoring erroneous data and invalid block types and the judgment of how to use error corrected data is left to the micro controller program.

TABLE 36 Last and Previous block type identification, read byte 4 and read byte 10

BLOCK TYPE IDENTIFICATION	LBI2 / PBI2	LBI1 / PBI1	LBI0 / PBI0
A	0	0	0
B	0	0	1
C	0	1	0
D	0	1	1
C'	1	0	0
valid E (RBDS mode)	1	0	1
invalid E (RDS mode)	1	1	0
invalid block type	1	1	1

TABLE 37 Last and Previous block corrected errors, read byte 4 and read byte 10

ERROR STATUS	ELB1 / EPB1	ELB0 / EPB0
reliable data: no errors found	0	0
less reliable data: up to 2 corrected bit errors	0	1
less reliable data: up to 5 corrected bit errors	1	0
erroneous data: uncorrectable bit errors	1	1

5.2.4 Synchronization flywheel

A synchronization search can be started at any time by setting of bit NWSY = 1, data byte 3H, however also an automatic detection of synchronization loss is possible by means of the flywheel function. This function starts a new synchronization search based on the number of valid blocks and invalid blocks received. The judgment of valid blocks and invalid blocks depends upon the setting of SYM controlling the error correction use (note this setting is also used during synchronization search).

TABLE 38 Setting of error correction use, byte 0H

BLOCK VALID JUDGMENT	SYM1	SYM0
only error free blocks	0	0
up to 2 corrected bit errors	0	1
up to 5 corrected bit errors	1	0
up to 5 corrected bit errors (only error free blocks during synchronization)	1	1

Furthermore the RBDS bit (data byte 1H) selects if E blocks are interpreted as valid blocks (RBDS mode) or invalid blocks (RDS mode).

When synchronization is established the TEF6892H keeps track of the number of received valid blocks (good blocks) and invalid blocks (bad blocks) by means of two counters; the good block counter and the bad block counter. The value of these counters can be read from bits GBC (good block counter, note that the GBC lsb value is not available via I^2C read), and bits BBC (bad block counter). The criterion that defines synchronization loss can be set by two values, GBL (good blocks lose) and BBL (bad blocks lose).

TABLE 39 Good block counter, read byte 9 and 10

GBC5, 4, 3, 2, 1 (0)	GOOD BLOCK COUNTER
0 - 62 (000000B - 111110B)	good block counter value

TABLE 40 Bad block counter, read byte 9

BBC5, 4, 3, 2, 1, 0	BAD BLOCK COUNTER
0 - 63 (000000B - 111111B)	bad block counter value

TABLE 41 Setting of maximum good blocks lose, byte 0H and byte 1H

GOOD BLOCKS LOSE	GBL5, 4, 3, 2, 1, 0
good block value for counter reset	0 - 63 (000000B - 111111B)

TABLE 42 Setting of maximum bad blocks lose, byte 1H

BAD BLOCKS LOSE	BBL5, 4, 3, 2, 1, 0
bad block value for new synchronization	0 - 63 (000000B - 111111B)

When the good block counter GBC reaches the GBL value both counters are reset to zero for a new count cycle, however when the bad block counter BBC reaches the bad block lose value set by BBL before that time a new synchronization is started. I.e. synchronization loss is detected when BBL is reached before GBL.
Another way of looking at these settings is that synchronization loss is assumed when the ratio of bad blocks compared to good blocks exceeds the setting of BBL over GBL, while the minimum detection speed is set by BBL. Usually an equal setting of BBL and GBL is used, this equals the definition of the SAA6588 flywheel function.

6. Power-On reset

The TEF689xH has a power on reset function. When the power supply is switched on, the write registers of the IC are in their default settings, which are described in Table 46. The device is in full stand-by mode and the four audio outputs are muted. When the supply voltage drops below 6.5 V during operation, the circuit is muted and reset to the power on reset state.

The power on reset status can be read out via I^2C bus with bit POR in read byte 1. POR = 0 indicates the continuous operation. If POR = 1, a power-on reset was detected since the last read cycle and a complete I^2C bus transmission is necessary for those bit settings different from default to set the IC to the desired continuous operation again.

The POR bit is reset to 0 after the read out. For initialization purposes the IC requires the 75.368 kHz reference frequency to be present. Should this not be the case the POR bit will not reset and remain 1 until a proper reference frequency is found.

The RDS decoder of the TEF6892H has an independent power on reset indication, if bit RSTD = 1 (read byte 4) a decoder reset is in progress.

7. Stand-by function

The IC can be set into stand-by, reducing current consumption.
Two stand-by modes are possible. The bits STBR and STBA control the stand-by function of the RDS part and the audio processing part.

In case of audio stand-by (STBA = 1) the fader mute function is activated automatically including ASI, the DC voltages at line inputs and outputs are preserved.

TABLE 43 Stand-by function, byte 4H

STBR	STBA	FUNCTION
0	0	complete circuit active
0	1	RDS processing active and audio processing stand-by
1	0	RDS processing stand-by and audio processing active
1	1	RDS processing and audio processing stand-by

8. The I^2C bus

All control of the TEF689xH is done via the I^2C-bus. The I^2C-bus interface can be operated with clock frequencies up to 400 kHz and is in full compliance with the ‘fast-mode’ I^2C specification. The I^2C-bus can be operated with a supply voltage ranging from 2.5 V to 5 V.

For detailed information see also the Philips Semiconductors document “The I^2C bus and how to use it”, document order no. 9398 393 40011.

A special feature of the TEF689xH is the I^2C gate, a controllable interface to a dedicated I^2C bus for the tuner IC. A supply voltage shift between main bus and tuner bus is supported within the 2.5 V to 5 V range.

8.1 Chip address

The TEF689xH can be used with two different chip addresses. The address is selected by the ADDR pin (pin 44, address select). When pin 44 is grounded the address is 30H, with pin 44 open the address is 32H.

8.2 Type identification

The different IC types of TEF6890H, TEF6892H and TEF6894H can be detected via I^2C by reading of the ID bits in read byte 1. This allows e.g. a micro controller to change between RDS functionality when different types of the TEF689xH series are used on the same board with the same micro controller program.

TABLE 44 Type identification, read byte 1

ID2	ID1	ID0	TYPE
0	0	0	TEF6890H
0	1	0	TEF6892H
1	0	0	TEF6894H

8.3 Auto increment function

The TEF6890H and TEF6894H have 18 write mode data bytes and the TEF6892H has a total of 21 write bytes to include RDS decoder control. The bytes are addressed by subaddresses. The first byte after the address byte includes the subaddress. Apart from the differences in RDS options the different IC types use the same I^2C structure for compatibility.

For an easier addressing of the subaddresses the auto-increment control can be used. The auto-increment control is enabled by bit AIOF in the subaddress byte. If AIOF = 0, the auto-increment is enabled.
With the auto-increment control the bus transmission starts with the subaddress value which is specified in the bits SA4 to SA0 in the subaddress byte. When more than one byte is sent to the TEF689xH, the subaddress is automatically incremented by 1 after receiving each byte. The subaddress value is incremented to subaddress 30 and then reverted to 0. The subaddress 31 (autogate control) can only be accessed by direct subaddress selection. From address 31 it is reverted to subaddress 0.
The TEF689xH does not use all possible subaddress numbers, but the auto-increment control counts also these numbers. That means that if a transmission includes unused bytes dummy bits have to be transmitted to address the correct bytes. For future compatibility it is advised to send 0 for unused bits.

A summary of the whole bus protocol is given in Table 45 to Table 48

TABLE 45 Write mode

S(1)	CHIP ADDRESS (write)	A(2)	SUBADDRESS	A(2)	DATA BYTE(S)	A(2)	P(3)

TABLE 46 Complete I2C bus protocol write mode (example of subaddress SA=1FH).

BYTE:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
address								
Address	0	0	1	1	0	0	ADDR	0
subaddress								
Subaddr.	AIOF	GATE	SGAT	SA4	SA3	SA2	SA1	SA0
default		0	0					
AUTOGATE								
1FH	AGA7	AGA6	AGA5	AGA4	AGA3	AGA2	AGA1	AGOF
default								1
RDS SET A (only used for TEF6892H)								
0H	0	SYM1	SYM0	GBL5	GBL4	GBL3	GBL2	GBL1
default	0	0	0	0	0	0	0	0
RDS SET B (only used for TEF6892H)								
1H	GBL0	RBDS	BBL5	BBL4	BBL3	BBL2	BBL1	BBL0
default	0	0	0	0	0	0	0	0
RDS CLK (CLKO and CLKI not used for TEF6894H)								
2H	0	0	TST3	TST2	TST1	TST0	CLKO	CLKI
default			0	0	0	0	0	1
RDS CONTROL (only used for TEF6892H)								
3H	DAC1	DAC0	NWSY	BBG4	BBG3	BBG2	BBG1	BBG0
default	0	0	0	0	0	0	0	0
CONTROL (STBR not used for TEF6894H)								
4H	STBR	STBA	AFUM	AFUH	RMUT	0	LETF	ATTB
default	1	1	0	0	0		0	0
CSALIGN								
5H	CSR1	CSR0	CSA3	CSA2	CSA1	CSA0	0	0
default	0	1	0	1	1	1		
MULTIPATH								
6H	USS1	USS0	WAS1	WAS0	LET1	LET0	MPT1	MPT0
default	0	1	0	1	0	0	0	0
SNC								
7H	SST3	SST2	SST1	SST0	SSL1	SSL0	HCMP	HCSF
default	0	1	1	1	0	1	0	0
HIGHCUT								
8H	HST2	HST1	HST0	HSL1	HSL0	HCF2	HCF1	HCF0
default	0	1	1	0	1	1	1	1
SOFTMUTE								
9H	MST2	MST1	MST0	MSL1	MSL0	UMD1	UMD0	SMON
default	0	1	1	0	1	0	1	1

BYTE:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RADIO								
AH	AM	MONO	DEMP	ING1	ING0	SEAR	NBS1	NBS0
default	0	0	0	0	0	1	1	0
INPUT/ASI								
BH	NBL1	NBL0	INP1	INP0	MUTE	ASI	AST1	AST0
default	0	0	0	0	1	1	0	0
LOUDNESS								
CH	0	LDN4	LDN3	LDN2	LDN1	LDN0	LLF	LHB
default		0	0	0	0	0	1	1
VOLUME								
DH	0	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
default		0	1	0	0	0	0	0
TREBLE								
EH	0	TRE2	TRE1	TRE0	TREM	TRF1	TRF0	0
default		0	0	0	1	0	1	
BASS								
FH	0	BAS2	BAS1	BAS0	BASM	BAF1	BAF0	BASH
default		0	0	0	1	1	0	0
FADER								
10H	0	0	FAD4	FAD3	FAD2	FAD1	FAD0	FADM
default			0	0	0	0	0	1
BALANCE								
11H	BAL6	BAL5	BAL4	BAL3	BAL2	BAL1	BAL0	BALM
default	0	0	0	0	0	0	0	1
MIX								
12H	MILF	MIRF	MILR	MIRR	MULF	MURF	MULR	MURR
default	0	0	0	0	1	1	1	1
BEEP								
13H	BEL2	BEL1	BEL0	BEF1	BEF0	NAV	0	0
default	0	0	0	0	0	0		
reserved								
14H-1EH	0	0	0	0	0	0	0	0

Notes

1. S = START condition
2. A = acknowledge (from TEF689xH)
3. P = STOP condition

TABLE 47 Read mode

S[1]	CHIP ADDRESS (read)	A[2]	DATA BYTE 1	A[4]	DATA BYTE(S)	A[4]	DATA BYTE	NA[5]	P[3]

TABLE 48 Complete I2C bus protocol read mode

BYTE:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
address								
Address	0	0	1	1	0	0	ADDR	1
data bytes (4 to 10 only used for TEF6892H)								
1	STIN	ASIA	AFUS	POR	–	ID2	ID1	ID0
2	LEV7	LEV6	LEV5	LEV4	LEV3	LEV2	LEV1	LEV0
3	USN3	USN2	USN1	USN0	WAM3	WAM2	WAM1	WAM0
4	SYNC	DOFL	RSTD	LBI2	LBI1	LBI0	ELB1	ELB0
5	LM15	LM14	LM13	LM12	LM11	LM10	LM9	LM8
6	LM7	LM6	LM5	LM4	LM3	LM2	LM1	LM0
7	PM15	PM14	PM13	PM12	PM11	PM10	PM9	PM8
8	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0
9	BBC5	BBC4	BBC3	BBC2	BBC1	BBC0	GBC5	GBC4
10	GBC3	GBC2	GBC1	PBI2	PBI1	PBI0	EPB1	EPB0

Notes

4. A = acknowledge (from master)
5. NA = not acknowledge (from master, signals end of read)

8.4 Gated I²C bus control of the tuner IC

The TEF689xH offers a gated I²C-bus connection to the tuner IC. The SDA- and SCL-pins of the tuner IC are not directly connected to the main bus of the radio, but via gates in the TEF689xH (SCLG and SDAG). The gates are only switched on, when a bus transmission to and from the tuner IC is intended. This avoids crosstalk of the bus pulses into the tuner circuit and thus reduces interference to the tuner. Furthermore since the gate function does not use switches but active buffer circuits the gated bus will show small interference by itself and the SDAG and SCLG pull up resistor value can be selected independently of the main I²C bus for lowest crosstalk.

The gate is enabled by the bit GATE in the subaddress byte. If GATE = 1, the I²C-bus gate to the tuner IC is enabled. If GATE = 0, the I²C-bus gate can be controlled by either the shortgate or the autogate function.

8.4.1 Shortgate

For the current NICE (TEA684xH) tuner series the shortgate function is the advised gate control. Shortgate opens the gate for the first following I²C transmission and closes the gate automatically afterwards. This way a minimum of control is required. The shortgate function is depicted in Fig.36

In part a. of Fig.36 the TEF689xH I²C gate is opened by setting SGAT = 1 in the subaddress byte. To avoid timing errors a start condition is generated to initialize activation of the I²C gate. This transmission can be transmitted at 400 kHz bus speed, also in case of a 100 kHz tuner like NICE. A standard I²C transmission can be used using a stop (P) condition or alternatively the following transmission can be linked using a repeated start (Sr). The use of a repeated start can be advantageous in case more then one micro controller can control the bus (multi master).

The next transmission (part b.) is the transmission to the tuner. This is the first transmission after activation of the shortgate function and this transmission will be available at the tuner I²C bus lines SDAG and SCLG. Of course

the maximum bus speed in this case is defined by the tuner.
At the stop (P) condition of this next transmission the gate will automatically close again.

Any following transmissions (part c.) will be blocked and can thus be transmitted at bus speeds up to 400 kHz.

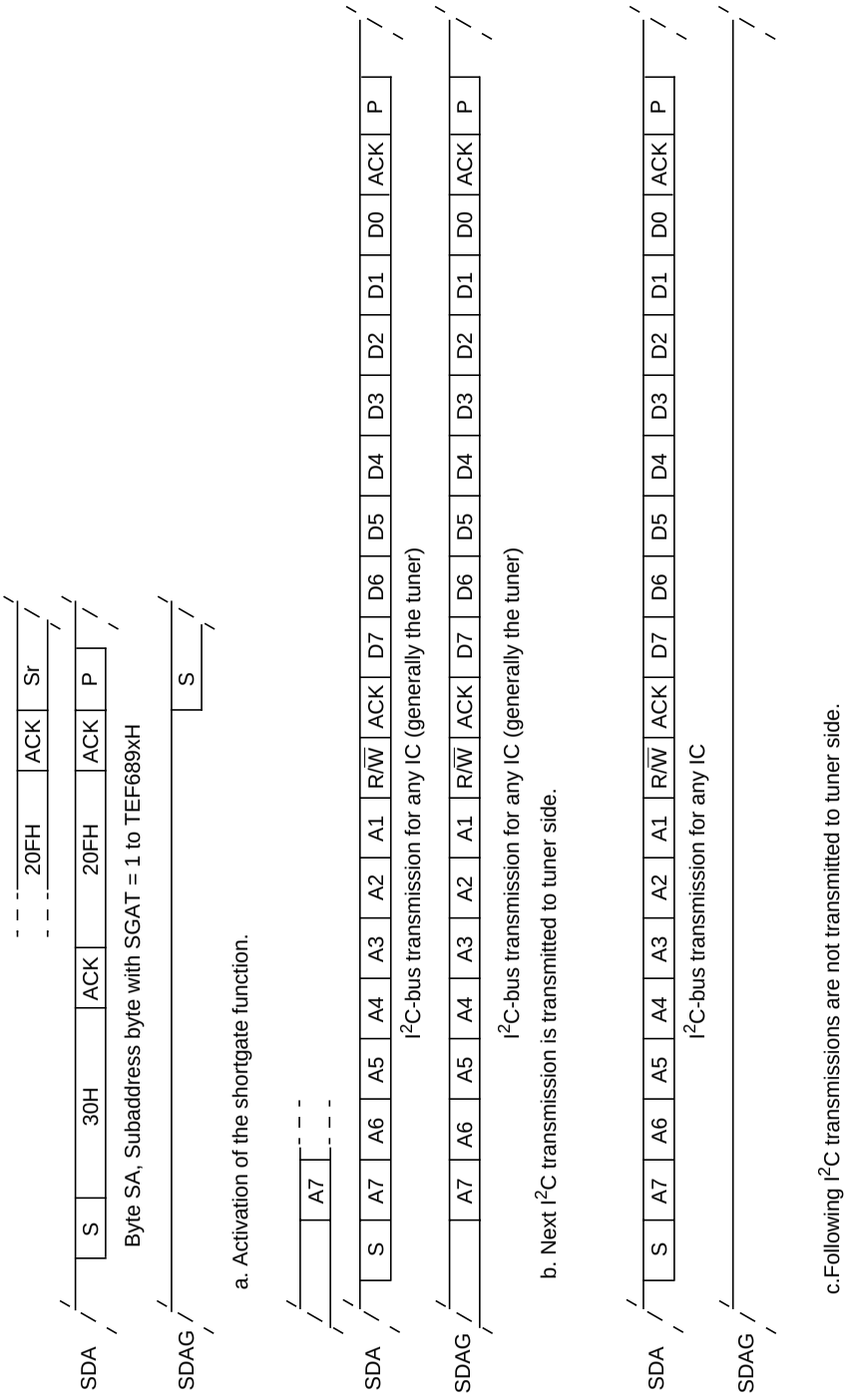


Fig.36 The shortgate function

8.4.2 Autogate

For future tuner series autogate will allow the most convenient control. Autogate opens the gate automatically when the tuner IC is addressed by the controller. This means for autogate there is no software control needed for the gate function, to the micro controller it seems as if the tuner IC is at the same bus as the TEF689xH. Autogate however can not be used with the NICE (TEA684xH) tuner series because IF counter reading may deliver erroneous results. The autogate function is described in Fig.37

In part a. of Fig.37 the address of the tuner IC is transmitted to the TEF689xH. This transmission contains the address of the TEF689xH, subaddress 31 and the tuner address together with bit AGOF = 0. Bit AGOF = 0 enables the autogate function. The TEF689xH sends the acknowledge and the tuner address is stored in the TEF689xH.

The next transmission (shown in part b.) on the main bus lets the TEF689xH send the tuner address to the tuner IC. While on the main bus SDA, SCL the address of one of the ICs is transmitted, the address of the tuner is sent on SDAG and SCLG. This transmission stops after AGA1. Now the tuner is partly addressed and is waiting for the last address bit (R/$\overline{W}$). The bus lines SDAG and SCLG are kept LOW for maximum noise immunity. (Note: Because the IF counter result of a NICE tuner is loaded immediately at transmission start the ‘early’ start of an autogate transmission may lead to false IF counter results.)

When the main controller addresses the tuner (part c.), the TEF689xH recognizes the first 7 bits of the tuner address and after the 7th bit opens the gate to the tuner. The tuner receives the R/$\overline{W}$ bit and sends the acknowledge to the main bus. During the following bytes the gate is open.

A next transmission will start as depicted in part b., partly addressing the tuner IC again. If this transmission does not contain the tuner IC address the gate is closed (SCLG and SDAG LOW) until reception of a tuner address.

Although the autogate function is restricted to detect only one address at a time it is possible to change the autogate address during use. A new transmission of part a. will define a new address, e.g. a RAM memory that is part of a tuner module. This address change can be performed on the fly, i.e. it is not required to disable and enable autogate (AGOF) to change the autogate address. Alternatively the GATE bit can be used to override autogate function. In any circumstance proper I^2C signals will be generated at the gated bus side to ensure correct control.

A special case is the situation where the main bus is desired to be run at high (400 kHz) speed and the tuner at standard (100 kHz) speed. The timing of the main bus is not only present for the gated transmissions but is also used for generation of the tuner address. Therefore the transmissions to the tuner (part c.) and the first byte of the following transmission (part b.) need to be run at the tuner I^2C speed. When using different bus speeds usage of the shortgate function is probably more convenient.

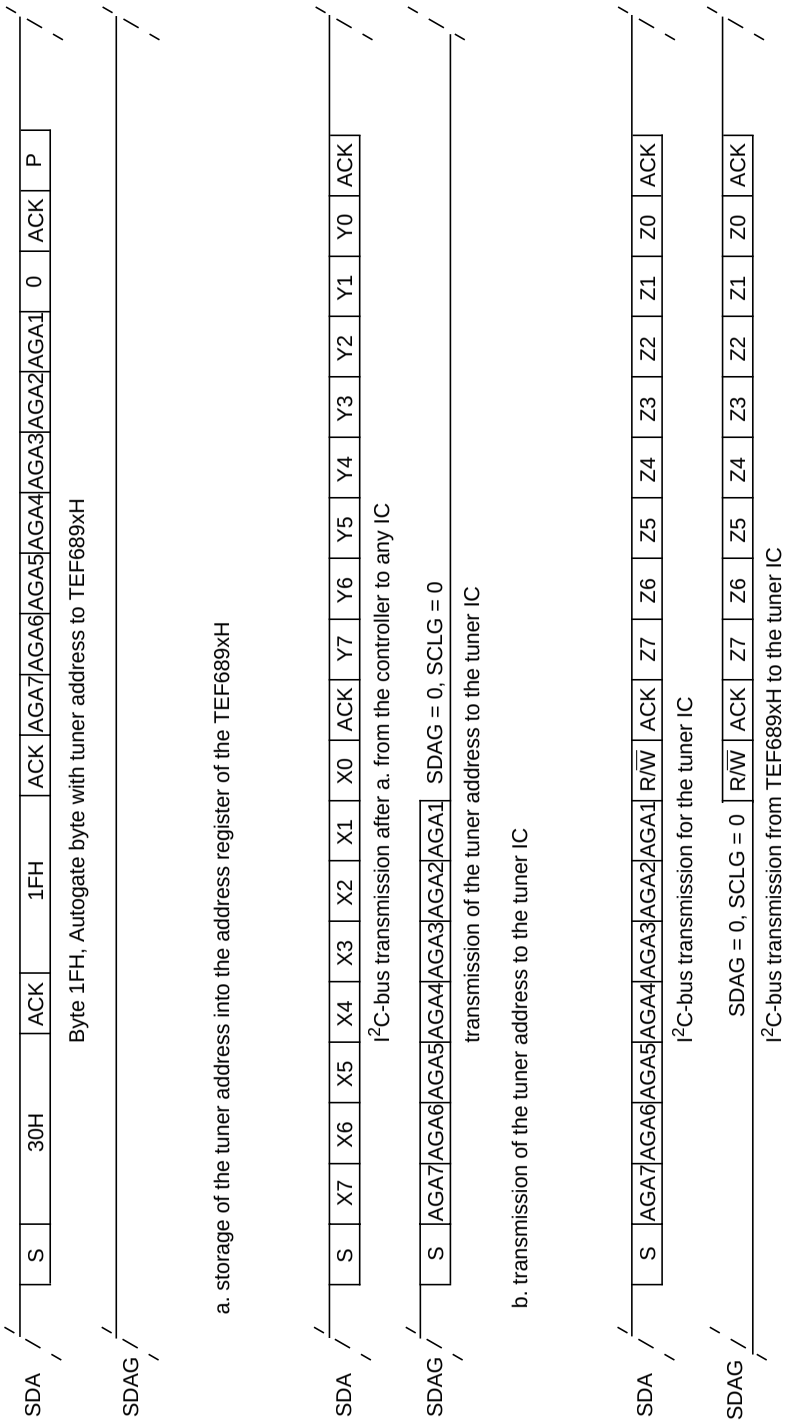


Fig.37 The autogate function

9. References

1. "The I^2C bus and how to use it", Philips Semiconductors. Document order no. 9398 393 40011
2. Data sheet TEF6890H, Philips Semiconductors
3. Data sheet TEF6892H, Philips Semiconductors
4. Data sheet TEF6894H, Philips Semiconductors